EXHIBIT C

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

STMICROELECTRONICS, INC.,

Petitioner,

v.

OCEAN SEMICONDUCTOR LLC,

Patent Owner.

IPR2021-01349

Patent No. 6,420,097 B1

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 6,420,097

(Claims 1-17)

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Ex. 1002	Declaration of John Bravman, Ph.D. ("Bravman Decl.")
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Ex. 1004	U.S. Patent No. 5,976,769 ("Chapman")
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Ex. 1006	U.S. Patent No. 6,362,111 ("Laaksonen")
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Ex. 1009	Q. Lin, et al., *Dual-layer inorganic SiON bottom ARC for 0.25-μm DUV hard mask applications*, Proc. SPIE 3678, Advances in Resist Technology and Processing XVI (June 11, 1999) ("Lin")
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Ex. 1021	R.A. Cirelli, et al., *A multilayer inorganic antireflective system for use in 248 nm deep ultraviolet lithography*, J. Vac. Sci. Technology B 14(6), Nov/Dec 1996 ("Cirelli")
Ex. 1022	Declaration of Rachel J. Watters regarding Lin
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Ex. 1024	T. Azuma, et al., *Impact of reduced resist thickness on deep ultraviolet lithography*, J. Vac. Sci. Technology B 14(6), Nov/Dec 1996 ("Azuma")

Ex. 1025	T. Ko, et al., *Implementation of organic bottom antireflective coating in 0.35-µm polycide fabrication*, Proc. SPIE 3183, Microlithographic Techniques in IC Fabrication (August 14, 1997) ("Ko")
Ex. 1026	Declaration of Patrick Franzen regarding Becker

I. INTRODUCTION

U.S. Patent No. 6,420,097 (the "'097 patent") is directed toward a method of creating narrower circuit structures, such as gate lines, than semiconductor patterning technology known as lithography would otherwise allow. To achieve that goal, the patent describes and claims using an intermediate hardmask layer between layers of photoresist and gate conductive material. Applying conventional etching techniques, that hardmask is narrowed or trimmed underneath the resist layer and acts as a mask for etching gate lines that are narrower than the original resist patterns produced by lithographic patterning.

Prior art not considered by the examiner during prosecution, however, shows that the alleged invention was not new. This Petition cites Chapman and Laaksonen as primary prior art references, both of which resulted from work at Texas Instruments. Each reference taught the intermediate hardmask layer described and claimed in the '097 patent. Likewise, each reference taught the etching techniques described in the patent to create smaller circuit structures, such as gate lines, based on a trimmed hardmask.

The other features recited in the claims of the '097 patent were well known and conventional in the art and would have been obvious to combine with the teachings of Chapman and Laaksonen. The '097 patent described an ultra-thin resist layer as prior art, as did Hause; Becker, Jeoung, and Wong all taught

techniques used to stabilize photoresist when etching an underlying film; and Lin and Cirelli each described a multilayered hardmask.

Based on prior art disclosures unknown to the examiner, claims 1-17 of the '097 patent are obvious over Chapman or Laaksonen in combination with other prior art.

II. MANDATORY NOTICES

A. Real Party-in-Interest

Petitioner STMicroelectronics, Inc. ("ST") is a real party-in-interest. Although STMicroelectronics N.V., ST's parent company, is not a real party-in-interest under the governing legal standard for making that determination, ST identifies it as a real party-in-interest for purposes of this Petition to avoid any disputes over that issue.

B. Related Matters

Ocean Semiconductor LLC ("Ocean") sued ST in the Western District of Texas, alleging infringement of the '097 patent, among other patents. *Ocean Semiconductor LLC v. STMicroelectronics, Inc.*, Case No. 6-20-cv-01215 (W.D. Tex.). ST was served with the complaint on January 5, 2021. Ocean Semiconductor has sued others alleging infringement of the '097 patent in two additional cases. One case is pending in the Western District of Texas (*Ocean Semiconductor LLC v. NXP Semiconductors NV*, Case No. 6-20-cv-01212 (W.D.

Tex.)) and the other in the District of Massachusetts (*Ocean Semiconductor LLC v. Infineon Techs. AG*, Case No. 1-20-cv-12311 (D. Mass.)).

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ST is concurrently filing an executed Power of Attorney appointing the above counsel.

III. GROUNDS FOR STANDING

ST certifies that the '097 patent is available for IPR and that ST is not barred or estopped from requesting review.

IV. IDENTIFICATION OF CHALLENGE AND RELIEF REQUESTED

ST requests cancellation of claims 1-17 based on the following grounds:

Ground	References	Basis	Claims
1	Chapman and AAPA[1] or Hause	§ 103	1-9, 16-17
2	Chapman, AAPA or Hause, and Becker or Jeoung or Wong	§ 103	10-11
3	Chapman, AAPA or Hause, and Lin or Cirelli	§ 103	12-15
4	Laaksonen and AAPA or Hause	§ 103	1-2, 4-9, 12-15, 17
5	Laaksonen, AAPA or Hause, and Chapman	§ 103	3, 16
6	Laaksonen, AAPA or Hause, Chapman, and Becker or Jeoung or Wong	§ 103	10-11

The Declaration of Dr. John Bravman (Ex. 1002) and evidence in the Exhibit List support this Petition. In addition, all grounds are supported by a skilled person's general knowledge. *Koninklijke Philips N.V. v. Google LLC*, 948 F.3d 1330, 1337-38 (Fed. Cir. 2020).

[1] Applicant Admitted Prior Art ("AAPA").

V. BACKGROUND

A. The '097 Patent

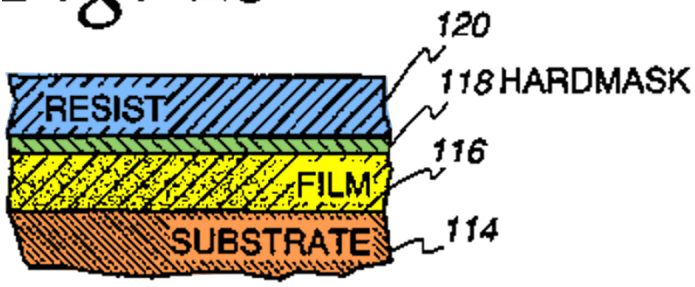
The '097 patent describes and claims a method for trimming a hardmask layer beneath photoresist through isotropic overetching during a process for manufacturing semiconductor circuit structures. As overall circuit size has decreased, the structural features in those circuits have also become smaller, including the linewidths of the gates that make up field-effect transistors or FETs. Ex. 1001, 1:10-20; Ex. 1002 ¶28. Gate linewidths depend on lithography techniques that create patterns for those structures. Ex. 1001, 1:16-20. Lithography uses carefully controlled wavelengths of light to expose photoresist materials to generate desired linewidth patterns. *Id.*; Ex. 1002 ¶27. At the time of the alleged invention, conventional lithography techniques and available light wavelengths were unable to produce resist and gate linewidths of less than about 2500Å. Ex. 1001, 1:29-32.

Using ultra-thin resist (UTR) layers was a known way to facilitate the manufacture of smaller circuits while maintaining desired characteristics, such as "near vertical sidewalls" and "maximum exposure/focus latitude." *Id.*, 1:32-43. But UTR layers led to problems—particularly when used in conjunction with trimming techniques for reducing linewidths of the resist and, by extension, underlying layers. *Id.*, 1:46-56. For example, the trim process consumed so much

resist that what remained of the UTR was insufficient to complete an acceptable etch of the underlying gate material. *Id.*, 1:50-54, 2:43-46, 3:33-53.

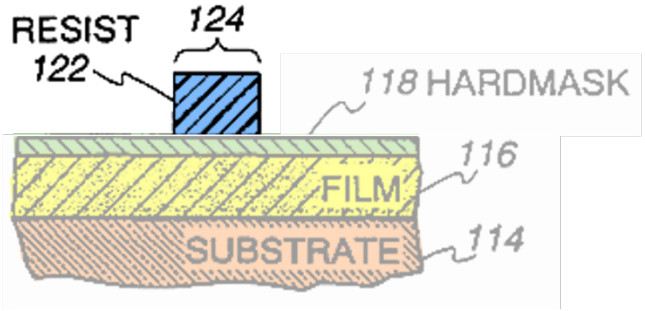
To allow for increasingly minute circuit structures, the '097 patent proposes using an intermediate hardmask layer between the resist layer and the layer of conductive material used to form gate lines. *Id.*, 1:60-63, 2:10-12. The layer stack is shown in annotated Figure 4b below. The stack includes UTR layer 120 (blue), hardmask layer 118 (green), gate conductive layer 116 (yellow), and substrate 114 (orange). *Id.*, 3:61-4:3.

Fig. 4b



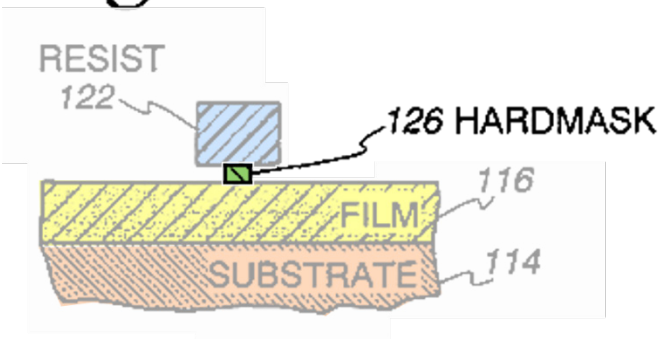
After forming the layer stack, patterning and etching the layers results in gate structures. First, UTR layer 120 "is patterned to a resist mask 122 [blue] which has an initial linewidth 124," as shown in annotated Figure 4(c) below. *Id.*, 4:14-16. Linewidth 124 "is assumed to be the smallest dimension obtained by image transfer from the UTR layer in the lithographic equipment." *Id.*, 4:16-18.

Fig. 4c



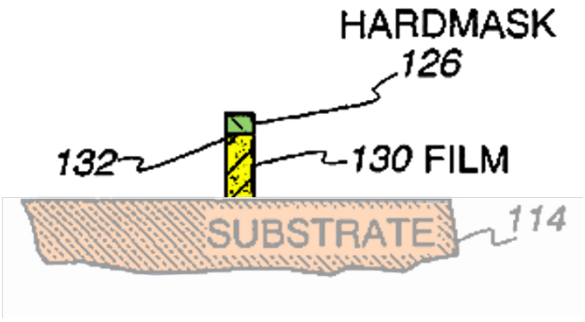
Next, hardmask 118 is etched anisotropically to remove the exposed portions of the hardmask and leave the portion that lies underneath resist mask 122. *Id.*, 4:67-5:5. Then hardmask 118 is "isot[r]opically over-etch[ed]" to trim away portions of the layer underneath resist mask 122 to form hardmask 126 (green), which is shown in annotated Figure 4d at right. *Id.*, 4:19-23; *see also id.*, 1:60-63. Significantly, the linewidth of hardmask 126 is narrower than the linewidth of resist mask 122. *Id.*, 4:23-26.

Fig. 4d



Annotated Figure 4f below shows that resist mask 122 has been removed and conductive gate layer 116 anisotropically etched using hardmask 126 (green) to form gate 130 (yellow). *Id.*, 2:18-21, 4:34-37. As a result of the hardmask trim process, the gate has a width substantially equal to the hardmask but narrower than the width that would have been possible using conventional lithographic techniques on their own. *Id.*, 2:18-21, 4:37-42, 5:9-16.

Fig. 4f



The '097 patent describes modifying this hardmask trim method by altering the resist layer, the hardmask layer, and the hardmask etch process, among other things. *Id.*, 4:43-5:8.

B. The Challenged Claims

Independent claim 1 includes a preamble that describes a method of forming circuit structures with linewidths smaller than those provided by conventional lithographic techniques. The method includes steps for forming a wafer stack with a "device layer" over a substrate, a hardmask layer over the device layer, and a UTR layer over the hardmask layer. The claim then recites forming a resist mask with an initial linewidth followed by three etching steps: (i) "anisotropically etching" exposed portions of the hardmask layer, (ii) "isotropically etching" the portion of the hardmask under the resist mask to create a hardmask with "a final linewidth which is narrower than the initial line width of the resist mask," and (iii) "anisotropically etching" the device layer to form a structure with the same linewidth as the hardmask.

Claims 2-17 depend, directly or indirectly, from claim 1 and add minor requirements. Claims 2 and 5-8 recite materials that make up specific layers. Claims 3-4 and 9 require certain layer thicknesses. Claims 10 and 11 describe using UV baking or electron beam curing techniques on the resist to "enhance selectivity" when etching the hardmask. Claim 12 describes a hardmask formed

from multiple layers. Claim 13 describes such a hardmask that includes a top anti-reflective layer and a bottom etchstop layer. Claim 14 requires forming the top anti-reflective layer from a nitride film, and claim 15 requires forming the bottom etchstop layer from an oxide film. Claims 16 and 17 relate to the resist mask. In claim 16, the mask is removed before the second anisotropic etch of claim 1; in claim 17, the mask remains during that etch.

C. Prosecution History

The '097 patent application was filed on May 2, 2000 and does not claim priority to any prior applications. The entire file history of the '097 patent comes to fewer than 100 pages. In the first Office Action, the examiner allowed three of the claims. Ex. 1003 at 54, 59. The examiner concluded the prior art failed to teach "prepar[ing] a device" using the claimed method with "three etching steps, an anisotropic etch of the hardmask layer, an isotropic etch of the hardmask, then an anisotropic etch of the underlying layers." *Id.* at 59. The examiner rejected the remaining claims based on the Yang, McKee, Lyons, and Downey references. *Id.* at 55-58. The applicant then amended several claims to depend from an allowed claim. *Id.* at 64. The examiner allowed those amended claims. *Id.* at 70-72.

D. Level of Skill in the Art

A person of ordinary skill in the art at the time of the alleged invention of the '097 patent ("skilled person") would have had (i) a Bachelor's degree in

chemical engineering, materials science, electrical engineering, physics, chemistry, or a similar field, and three or four years of work experience in integrated circuit fabrication or related fields; or (ii) a Master's degree in the technical areas listed above, and two or three years of work experience in semiconductor manufacturing or related fields; or (iii) a Ph.D. in the technical areas listed above. Ex. 1002 ¶22.

E. Claim Construction

Claim terms in an IPR are construed "in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent." 37 C.F.R. § 42.100(b). For purposes of this proceeding, ST gives claim terms their plain and ordinary meaning. ST does not propose any express claim constructions because none is necessary for the Board to determine whether to institute review and cancel the challenged claims. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co. Matal*, 868 F.3d 1013, 1017 (Fed. Cir. 2017).

VI. THE CHALLENGED CLAIMS ARE UNPATENTABLE

A. Overview of the Prior Art

The claimed methods of the '097 patent were not new as of November 7, 1999, the date on which Ocean alleges it was conceived.[2] Ex. 1011 at 12. Multiple references show that the methods were known in the prior art before then.

1. The prior art taught trimming a hardmask using the three claimed etching steps

The '097 patent touts the alleged invention as trimming a hardmask between a resist mask and a gate conductive layer to achieve linewidths for circuit structures like gates that are narrower than linewidths provided by conventional lithography techniques. Ex. 1001, 1:57-63, 5:9-15. To accomplish that trimming, the patent describes and claims a three-step etching process: (i) anisotropically etching a hardmask layer to remove portions not covered by a resist mask, (ii) isotropically etching the remaining hardmask underneath the resist mask, and (iii) anisotropically etching the underlying gate conductive layer to remove

[2] ST reserves the right to argue that the claims of the '097 patent are not entitled to an invention date of November 7, 1999.

material not covered by the hardmask. *Id.*, 4:19-42. The examiner identified these three steps as the reason for allowing the claims. Ex. 1003 at 71.

But circumventing the limits of lithographic tools by using a hardmask to reduce circuit structure linewidths was not a new idea. Well before November 7, 1999, several prior art references taught doing so using the same three-step etching process that the examiner believed to be inventive. Ex. 1002 ¶¶27-31.

a. Chapman

U.S. Patent No. 5,976,769 to Richard Chapman ("Chapman") was filed on July 12, 1996 and issued on November 2, 1999. Ex. 1004. Texas Instruments was the original assignee of the patent. *Id.* Chapman pre-dates the '097 patent's alleged invention date of November 7, 1999 and therefore qualifies as prior art under 35 U.S.C. § 102(a) and (e).[3] Chapman was not before the examiner during prosecution of the '097 patent.

Just as in the '097 patent, to achieve "sublithographic patterns," Chapman taught using "an intermediate layer between photoresist and material to be etched together with lateral etching of … the intermediate layer to shrink the linewidth." Ex. 1004, 1:57-61. Chapman further taught the same three steps as described in

[3] References to 35 U.S.C. §§102, 103, and 119 are to their pre-AIA versions.

the '097 patent: (i) "an anisotropic etch to remove the exposed portions" of a hardmask layer (*id.*, 5:40-41), (ii) "a timed isotropic etch to laterally remove" a portion of the hardmask layer (*id.*, 5:49-52), and (iii) "anisotropically etch[ing]" an underlying polysilicon layer using the hardmask (*id.*, 5:63-65). Annotated Figures 8d and 8e below show the trimmed hardmask and resulting etched polysilicon. The figures illustrate resist (blue), hardmask (green), polysilicon (yellow), and substrate (orange) materials.

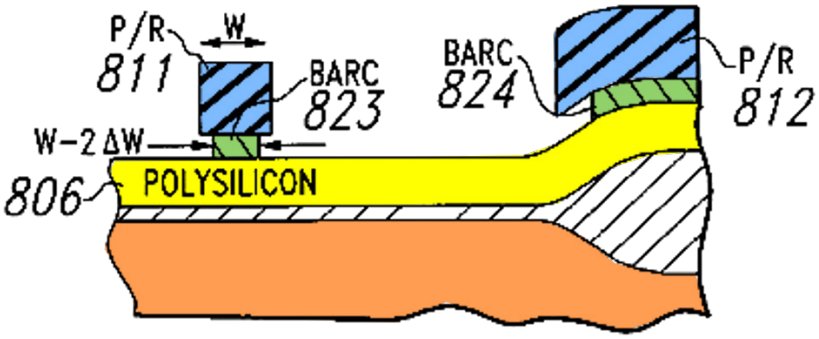


Fig. 8d

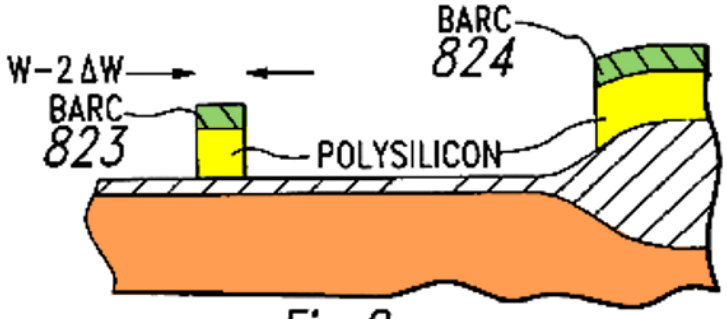


Fig. 8e

b. Laaksonen

U.S. Patent No. 6,362,111 to Reima Laaksonen, et al. ("Laaksonen") was filed on August 25, 1999 and issued on March 26, 2002. Ex. 1006. The patent

was assigned to Texas Instruments. *Id.* Laaksonen claims priority to U.S. Provisional Application No. 60/111,465 filed on December 9, 1998 ("'465 application"). Ex. 1012. As explained below, Laaksonen is prior art as of the December 9, 1998 filing date of the '465 application. Therefore, Laaksonen predates the '097 patent's alleged invention date of November 7, 1999, and qualifies as prior art under at least 35 U.S.C. § 102(e). Laaksonen was not before the examiner during prosecution of the '097 patent.

Like Chapman, Laaksonen disclosed a "process for forming a polysilicon line having linewidths below the lithography tool limits" by inserting a hardmask layer (a bottom anti-reflective coating (BARC)) between resist and polysilicon layers and then horizontally etching the hardmask layer to trim it. Ex. 1006, 1:52-67; *see also id.*, 2:34-53. Laaksonen also taught using the claimed etching steps to obtain narrower linewidths. First, the BARC layer is etched anisotropically in the vertical direction to remove the portions of that layer not covered by resist. *Id.*, 3:30-34. Second, an isotropic overetch process introduces a "horizontal component" to the etch that reduces the width of the BARC layer and the overlying resist. *Id.*, 3:34-66. Finally, the polysilicon layer under the BARC mask is etched anisotropically in the vertical direction, resulting in polysilicon lines having the same width as the BARC hardmask. *Id.*, 4:18-19, 4:33-35, Figs. 5-6. Annotated Figure 1 below shows that resist pattern 40 (red dashed line), which

has an initial width of L_P (red arrows and text), and BARC layer 30 are both trimmed to a reduced width of L_{RW}. *Id.*, 2:34-53. The figure shows resist (blue), hardmask (green), polysilicon (yellow), and substrate (orange) materials.[4]

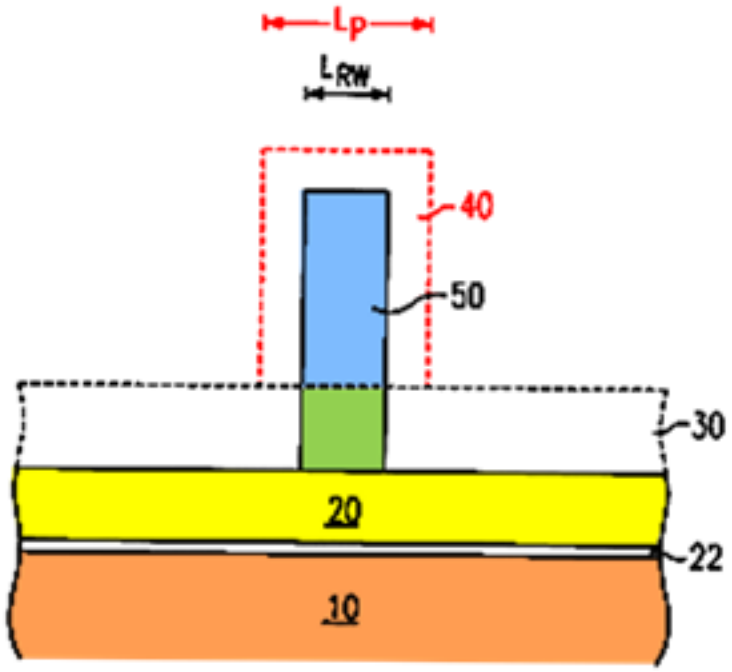


FIG. 1

[4] Another earlier-filed Texas Instruments patent, U.S. Patent No. 6,010,829 to Daty Michael Rogers, et al. ("Rogers"), includes teachings nearly identical to those found in Laaksonen. Ex. 1005, 1:38-53, 2:36-57, 3:36-67, Fig. 1. Rogers is another example of prior art that taught the claimed hardmask trim and etching steps.

2. Other claimed features were already known in the prior art

The '097 patent also describes and claims additional techniques that were already taught in the prior art to provide previously known benefits. Ex. 1002 ¶¶ 26-37.

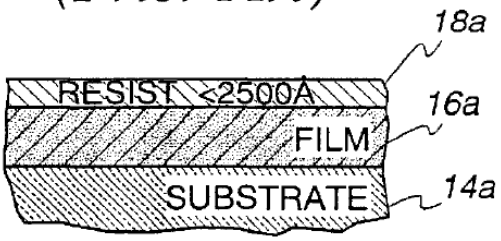
a. Hause

U.S. Patent No. 5,885,887 to Frederick Hause, et al. ("Hause") was filed on April 21, 1997 and issued on March 23, 1999. Ex. 1007. Because Hause's issuance date precedes the '097 patent's filing date of May 2, 2000 by more than one year, the reference qualifies as prior art under at least 35 U.S.C. § 102(b). Although Hause was identified as prior art during prosecution, the examiner did not rely on it for any rejections or analyze its teachings. Ex. 1003 at 61-62.

Hause taught using a UTR having a thickness of 2000Å. Ex. 1007, 4:14-17, 4:24-26. Hause described that a UTR layer was beneficial because it "replicates an image pattern more accurately than thicker photoresist layers" leading to, for example, "an accurately defined length" when etching an underlying layer. *Id.*, 2:40-50; *see also id.*, 4:24-26 ("Of importance, photoresist layer 114 is an ultra-thin layer that replicates the first image pattern with a high degree of accuracy.").

The '097 patent itself recognizes that UTR layers were known at the time of the alleged invention and provided improved patterning, including "near vertical sidewalls for the resist profiles" and "maximum exposure/focus latitude." Ex. 1001, 1:29-43. Figure 2a, at right, which is labeled "Prior Art," shows a UTR layer with a thickness of "<2500Å."

Fig. 2a
(Prior Art)



b. Becker, Jeoung, and Wong

Gerry Becker, et al., prepared a paper, *A comparative study of resist stabilization techniques for metal etch processing* ("Becker"), for SPIE's Conference on Advances in Resist Technology and Processing XVI in March 1999. That paper was published at pages 1126-1135 of Volume 3678 of the Proceedings of SPIE on June 10, 1999. Ex. 1008; Ex. 1026 ¶9. Becker was published and available to the public no later than August 11, 1999, several months before the '097 patent's alleged invention date of November 7, 1999. Ex. 1008; Ex. 1010 at 2; Ex. 1026 ¶9. Becker is therefore prior art under 35 U.S.C. § 102(a). U.S. Patent No. 6,358,672 to Gyu-chan Jeoung, et al. ("Jeoung") was filed on November 16, 1998 and issued on March 19, 2002. Ex. 1019. U.S. Patent No. 6,319,655 to Selmer Wong and Matthew Ross ("Wong") was filed on June 11, 1999 and issued on November 20, 2001. Ex. 1020. Because Jeoung's and

Wong's filing dates fall before the alleged invention date of November 7, 1999, both references qualify as prior art under at least 35 U.S.C. § 102(e). Becker, Jeoung, and Wong were not before the examiner during prosecution of the '097 patent.

Becker disclosed using two known techniques for processing a resist material—ultraviolet (UV) baking and curing using an electron beam. Ex. 1008 at 1126-27. These approaches improved the resist by stabilizing it before subsequent etching, making the etch more selective to a layer under the resist. *Id.* at 1126-29, 1133-34; Ex. 1002 ¶¶ 89-90. Jeoung and Wong taught the same techniques. Jeoung disclosed UV baking a photoresist that serves as an etching mask to increase its stability. Ex. 1019, 8:36-41, 9:36-42. Wong described exposing a resist to an electron beam, which made the resist more stable and decreased its etching rate. Ex. 1020, 8:37-40, 9:59-62, 11:60-67. Wong further taught applying the technique to photoresist with a thickness corresponding to a UTR layer. Ex. 1020, 7:7-10.

c. Lin and Cirelli

Qunying Lin and others wrote a paper, *Dual-layer inorganic SiON bottom ARC for 0.25-μm DUV hard mask applications* ("Lin") for SPIE's Conference on Advances in Resist Technology and Processing XVI in March 1999. That paper was published at pages 186-197 of Volume 3678 of the Proceedings of SPIE on

June 10, 1999. Ex. 1009; Ex. 1014 ¶9. Lin was published and available to the public no later than August 11, 1999, several months before the '097 patent's alleged invention date of November 7, 1999. Ex. 1009; Ex. 1022 at 2; Ex. 1014 ¶9. Lin is therefore prior art under 35 U.S.C. § 102(a). Lin was not before the examiner during prosecution of the '097 patent.

Lin taught a hardmask layer that includes multiple layers. Specifically, the hardmask includes a top SiON BARC layer having two sublayers and a bottom layer made from oxide or nitride. Ex. 1009 at 186-88, 191-92. Lin described that the multilayered hardmask simplifies manufacturing by reducing the need to tightly control the thickness of the various hardmask layers and provides better performance. *Id.* at 186, 196.

R.A. Cirelli, et al. published a paper entitled *A multilayer inorganic antireflective system for use in 248 nm deep ultraviolet lithography* ("Cirelli") at pages 4229-33 of Volume 14, No. 6 of the Journal of Vacuum Science & Technology B in "Nov/Dec 1996." Ex. 1021. Cirelli was published and publicly available no later than January 1997—over a year before the '097 patent's filing date of May 2, 2000. Ex. 1021; Ex. 1023 at 2. Cirelli is therefore prior art under at least 35 U.S.C. § 102(b). Cirelli was not before the examiner during prosecution of the '097 patent.

Like Lin, Cirelli disclosed a multilayered hardmask. Cirelli taught a hardmask with a nitride-based "ARC" or anti-reflective coating layer stack on top of an oxide layer. Ex. 1021 at 4230-31, 4233. This multilayered hardmask prevented reflection and its harmful effects without requiring the detailed thickness control necessary for a single-layered hardmask. *Id.* at 4229-31. The disclosed hardmask also provided "[e]xcellent imaging and etch performance" and "superb linewidth control." *Id.* at 4233.

B. Laaksonen is entitled to the benefit of the '465 application's filing date

As described in the chart below, the written description of the '465 application provides support for claim 9 of Laaksonen. Ex. 1002 ¶81. Moreover, the written description of the '465 application provides support for disclosures from Laaksonen that ST relies on below to show that claims 1-17 of the '097 patent are obvious. *Id*. For these reasons, Laaksonen is entitled to the benefit of the filing date of the '465 application (December 9, 1998) under 35 U.S.C. § 119(e)(1) and is prior art under at least 35 U.S.C. § 102(e) as of that date. *See Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1381 (Fed. Cir. 2015); MPEP § 2136.03(III).

Laaksonen Claim 9	**Written description support in '465 application (Ex. 1012)**
A method of fabricating an integrated circuit, comprising the steps of:	*E.g.*, 1:5-6, 3:4-5, claim 10
depositing a layer of polysilicon;	*E.g.*, 3:4, 5:23-24, claim 10
depositing a layer of bottom anti-reflective coating (BARC) over the polysilicon layer;	*E.g.*, 3:5, 6:4-5, claim 10
depositing a layer of resist over said BARC layer;	*E.g.*, 6:6-7, claim 10
removing portions of said resist layer to create a resist pattern using a lithographic tool;	*E.g.*, 3:5-7, 7:2-6, claim 10
etching said BARC layer with an etch chemistry comprising HBr/O_2 using said resist pattern until an end-point is detected and then continuing the etch for a selected time to overetch said BARC layer and said	*E.g.*, 3:8-11, 3:15-16, 7:8-19, 9:3-10, claim 10

resist pattern, wherein said overetch has a selectivity between the BARC layer and the resist pattern of approx-imately one to one such that a re-duced width pattern having a width less than 0.20 μm is created;	
etching said polysilicon layer using said reduced width pattern to create a polysilicon line.	*E.g.*, 3:12-13, 8:8-13, claim 10
Laaksonen (Ex. 1006) Disclosures	**Written description support in '465 application (Ex. 1012)**
1:10-12	1:5-6
1:34-36	2:2-3
1:52-2:5	3:3-16
2:28-29	5:3-4
2:34-3:3	5:8-6:8
3:8-15	6:15-19
3:24-67	7:2-16
4:3-9	7:21-24

4:17-27	8:8-14
4:30-37	8:16-20
4:67-5:5	9:25-10:4
5:11-14	10:9-11
5:19-20	10:14-15
5:27-30	10:18-22
Figs. 1-6	Figs. 1-6

C. Ground 1: Chapman and AAPA or Hause render obvious claims 1-9 and 16-17

As described above (at 12-13), Chapman disclosed the hardmask layer and etching steps claimed in the '097 patent. Chapman also disclosed all other aspects of claims 1-9 and 16-17, except for a UTR layer. But Applicant Admitted Prior Art ("AAPA") and Hause both disclosed a UTR layer. A skilled person would have been motivated to augment Chapman's teachings with AAPA or Hause's disclosures, and together the art renders claims 1-9 and 16-17 obvious.

1. Claim 1:

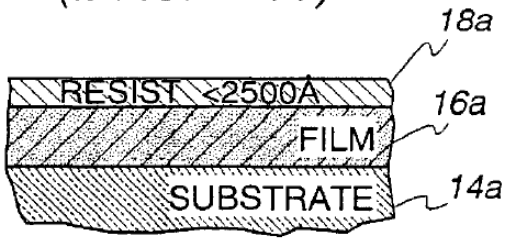
a. 1[pre]: *A method of forming circuit structures having linewidths which are smaller than what is achievable by conventional UV lithographic techniques on ultra-thin resist layers, said method comprising the steps of:*

To the extent the preamble is limiting, Chapman and AAPA or Hause render it obvious. Chapman taught a method for "fabrication" of "semiconductor

devices" that provides "sublithographic patterns." Ex. 1004, 1:10-12, 1:57-67. The method "shrink[s] the linewidth" of circuit structures despite the limits of the lithography tools available at the time. *Id.*, 1:27-34, 1:57-61. The disclosed technique involves a resist. *Id.*, 1:57-61.

The preamble of claim 1 requires a UTR layer. The '097 patent describes a UTR layer as having a thickness under 2500Å. Ex. 1001, 1:43-45. It would have been obvious to use a UTR layer in Chapman's method based on AAPA and/or Hause. For one, the patent describes that UTR layers, and the benefits associated with them, were generally known in the art at the time of the alleged invention. The patent recognizes in its "Background of the Invention" section that UTR layers "ha[d] been developed" before the time of the invention (*id.*, 1:34-39) and, as shown in Figure 2a at right, expressly characterizes resist layers of "<2500Å" as "Prior Art."

Fig. 2a
(Prior Art)



The AAPA disclosures in the '097 patent, and the similar disclosures in several prior art references, confirm that UTR layers were generally known to skilled artisans. Ex. 1002 ¶¶32-34. That fact is relevant to the obviousness determination here. *Koninklijke*, 948 F.3d at 1337. Indeed, the Patent Office has described that AAPA relating to a skilled person's general knowledge can

"supply[] missing claim limitations that were generally known in the art prior to the invention." USPTO Memorandum on the Treatment of Statements of the Applicant in the Challenged Patent in Inter Partes Reviews under § 311[5] ("AAPA Memo") at 9. The '097 patent describes general knowledge that includes the claimed UTR layer. Ex. 1002 ¶¶38-43. Moreover, those same disclosures supply "a motivation to combine particular disclosures." AAPA Memo at 9. A skilled person would have used a UTR layer in Chapman's method to obtain the known benefits described in the patent. UTRs overcame drawbacks with "classic image exposure techniques," including by "maintain[ing] the desired characteristics of the masked photoresist structures (e.g., near vertical sidewalls for the resist profiles, maximum exposure/focus latitude)." Ex. 1001, 1:29-39. These "desired characteristics" would have made it easier to use etching to replicate a photoresist pattern in an underlying layer. Ex. 1002 ¶103.

Separately, other prior art disclosed UTR layers. For example, Hause taught such a layer. Ex. 1007, 4:14-17 ("photoresist layer 114 has a thickness of merely 2000 angstroms"). Based on those teachings, a skilled person would have used a UTR layer in Chapman's method. Ex. 1002 ¶¶102-05. Chapman disclosed

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[5] Available at https://go.usa.gov/xAEdJ.

a resist with a thickness of 10000Å (Ex. 1004, 5:30-33), but suggested that "layer thicknesses … could all be varied" (*id.*, 6:64-66). Hause explained why using a UTR layer would have been beneficial: a photoresist "thickness on the order of 8000 to 10,000 angstroms" "may be too large to accurately replicate the image pattern." Ex. 1007, 2:22-25. Hause further disclosed that using its UTR layer having a 2000Å thickness would have avoided that issue because the layer "replicates an image pattern more accurately than thicker photoresist layers." *Id.*, 2:40-44; *see also id.* 4:25-27 ("photoresist layer 114 is an ultra-thin layer that replicates the first image pattern with a high degree of accuracy"). A UTR layer allows for underlying structures with, for example, "accurately defined length[s]." *Id.*, 2:44-50. Chapman's photoresist has a thickness that falls within the problematic range identified in Hause. A skilled person would have combined Chapman and Hause to improve Chapman's photoresist by obtaining the accuracy advantages of the UTR layer taught in Hause. Ex. 1002 ¶¶106-07. It was also known in the art that UTR layers facilitated better process control, which provided yet another motivation to use them. Ex. 1024 at 4251; Ex. 1002 ¶104.

b. 1[a]: *providing a semiconductor wafer stack formed of a substrate and a device layer above the substrate;*

Chapman taught a semiconductor device having different layers, including gate level polysilicon layer 806 (yellow) above silicon substrate 802 (orange), as shown in annotated Figure 8a below. Ex. 1004, 5:17-20.

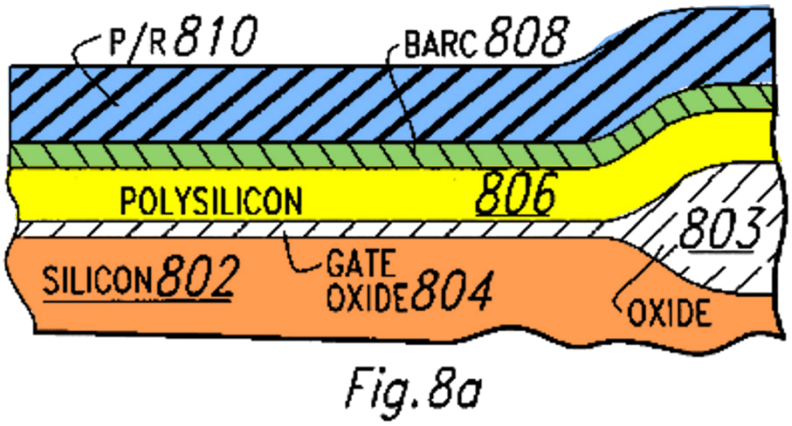
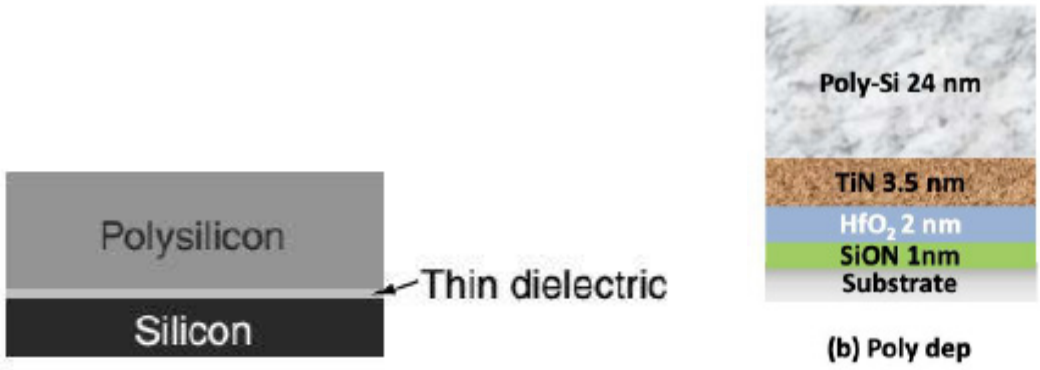


Fig. 8a

The '097 patent describes the claimed "device layer" as a "gate conductive layer" (Ex. 1001, 3:63-65) made from silicon (claim 2). Chapman's "***gate*** level ***polysilicon*** layer" has the same characteristics—it is used to form gates and is made from silicon. Ex. 1004, 2:52-55, 5:15-20; Ex. 1002 ¶108. Chapman's polysilicon layer is the same as the "device layer" disclosed in the patent. Ex. 1002 ¶109.

Further, in co-pending litigation, Ocean argues that a wafer stack that includes one or more oxide layers between the substrate and device layers, as shown in the figures below, infringes this limitation. Ex. 1013 at 6, 8. Under Ocean's interpretation of this limitation, Chapman's gate level polysilicon layer 806 is "above" substrate 802, despite the presence of gate oxide 804.



c. 1[b]: *depositing a hardmask layer over the device layer;*

Chapman disclosed BARC layer 808 (green) deposited over polysilicon layer 806 (yellow)—the "device layer," as shown in annotated Figure 8a above. Ex. 1004, 5:23-29. BARC layer 806 is used as a "final etch mask" when etching polysilicon layer 808. *Id.*, 5:59-62; Ex. 1002 ¶¶110-11. The '097 patent describes BARC as an example of a hardmask layer. Ex. 1001, 4:4-8.

d. 1[c]: *depositing an ultra-thin resist layer over the hard-mask layer;*

The layer stack in Chapman includes photoresist layer 810 (blue) deposited over BARC layer 808 (green), as shown in annotated Figure 8a above. Ex. 1004, 5:30-33. In addition, as described above (at 24-26), a skilled person would have been motivated to use the UTR layer taught in the prior art in combination with Chapman's method. Ex. 1002 ¶¶112-13.

e. 1[d]: *forming a resist mask having an initial linewidth;*

Chapman taught patterning photoresist layer 810 to form patterned photoresist portions 811 and 812 (blue), as shown in annotated Figure 8b below.

Ex. 1004, 5:36-41. The resist portions act as a mask when etching BARC layer 808 (green). Ex. 1004, 5:36-41; Ex. 1002 ¶114. The resist mask portion 811 has an initial linewidth labeled "W." Ex. 1004, 5:38-39.

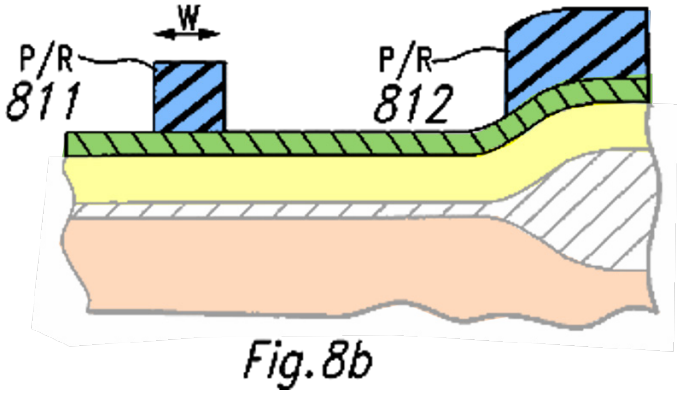
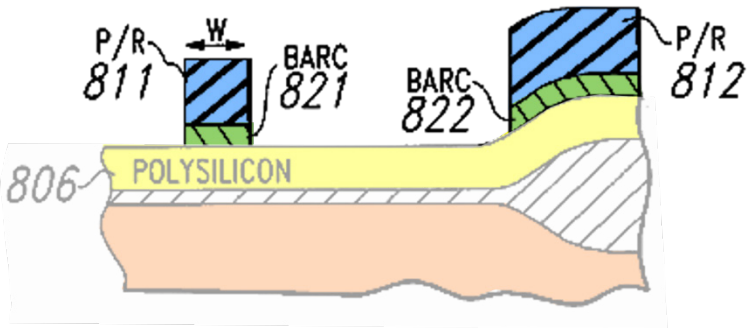


Fig. 8b

f. 1[e]: *anisotropically etching exposed portions of the hardmask layer;*

Chapman disclosed "applying an anisotropic etch to remove the exposed portions of BARC layer 808." Ex. 1004, 5:40-45. Annotated Figure 8c below shows BARC portion 821 (green), which remains after the etch. Ex. 1002 ¶115.



g. 1[f]: *isotropically etching subsequently the hardmask layer underneath the resist mask to form a hardmask having a final linewidth which is narrower than the initial line width of the resist mask and corresponds to a desired structure linewidth; and*

After the anisotropic etch of the BARC hardmask layer, Chapman taught "[a]pply[ing] a timed isotropic etch to laterally remove" some of BARC portion 821. Ex. 1004, 5:49-52. The resulting narrowed BARC portion 823 (green) is shown below in annotated Figure 8d. Narrow BARC portion 823 has a linewidth of 0.25 µm (labeled "W – 2 ΔW") that is narrower than the initial width of 0.30 µm (labeled "W") for photoresist portion 811 (blue). *Id.*, 5:38-39, 5:49-52. Narrowed BARC portion 823 "forms the final etch mask with W – 2 ΔW minimum linewidth to be used for anisotropic etching of polysilicon 806" (yellow). *Id.*, 5:59-62. That final etch mask provides the desired linewidth of polysilicon 806. *Id.*, Fig. 8e; Ex. 1002 ¶¶ 116-18.

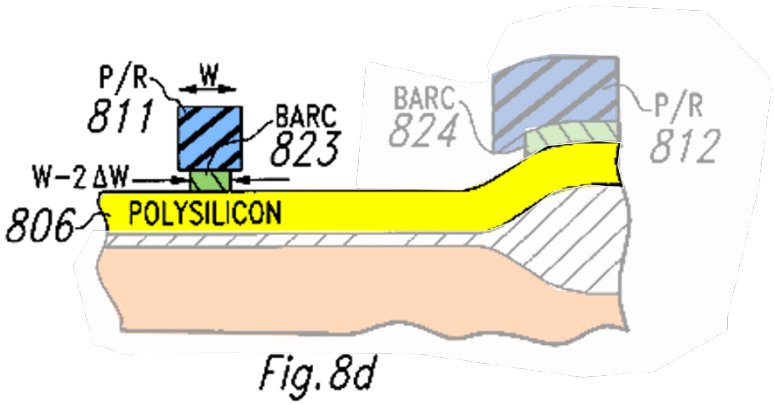


Fig. 8d

h. 1[g]: *anisotropically etching the device layer as defined by the hardmask to form a structure having a width substantially equal to the final linewidth of the hardmask.*

Following the isotropic etch of the BARC material, Chapman disclosed "anisotropically etch[ing]" polysilicon 806—the "device layer"—using narrowed BARC portion 823 (green)—the "hardmask"—as an etch mask. Ex. 1004, 5:63-65. The result is shown in annotated Figure 8e below. The polysilicon structure formed by this step (yellow) has a linewidth of "W – 2 ΔW," which is the same as the linewidth of narrowed BARC portion 823 (green). Ex. 1002 ¶119.

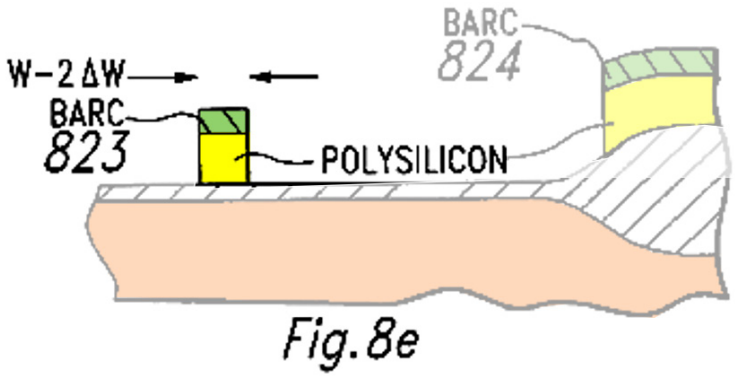


Fig. 8e

2. **Claim 2:** *A method of forming circuit structures as claimed in claim 1, wherein the device layer is formed of silicon.*

As described above, Chapman and AAPA or Hause render claim 1 obvious. The combination also renders claim 2 obvious. Chapman taught that "gate level polysilicon layer 806"—the "device layer"—is formed of polysilicon, a polycrystalline form of silicon. Ex. 1004, 5:17-20; Ex. 1002 ¶¶120-21.

3. **Claim 3:** *A method of forming circuit structures as claimed in claim 2, wherein the silicon has a thickness between 500 Å to 5000 Å.*

As described above, Chapman and AAPA or Hause render claim 2 obvious. The combination also renders claim 3 obvious. Polysilicon layer 806 disclosed in Chapman has a thickness of 400 nm, which is equal to 4000Å. Ex. 1004, 5:17-20; Ex. 1002 ¶¶ 122-23.

4. **Claim 4:** *A method of forming circuit structures as claimed in claim 1, wherein the ultra-thin resist layer has a thickness of less than 2500 Å.*

As described above, Chapman and AAPA or Hause render claim 1 obvious. As further described above (at 24-26), that combination would have included the UTR layer taught in the prior art having a thickness less than 2500 Å.

5. **Claim 5:** *A method of forming circuit structures as claimed in claim 4, wherein the hardmask is made of an inorganic material.*

As described above, Chapman and AAPA or Hause render claim 4 obvious. The combination also renders claim 5 obvious. Chapman disclosed a BARC layer—the "hardmask layer"—made from titanium nitride (TiN). Ex. 1004, 5:23-24. As described in the '097 patent, TiN is an "inorganic" material. Ex. 1001, 4:4:4-7, claim 6; Ex. 1002 ¶¶ 125-26.

6. **Claim 6:** *A method of forming circuit structures as claimed in claim 5, wherein the inorganic material is one of silicon dioxide, silicon nitride, silicon oxynitride, and titanium nitride.*

As described above, Chapman and AAPA or Hause render claim 5 obvious. The combination also renders claim 6 obvious. Chapman disclosed using titanium nitride to form the BARC layer. Ex. 1004, 5:23-24; Ex. 1002 ¶¶ 127-28.

7. **Claim 7:** *A method of forming circuit structures as claimed in claim 4, wherein the hardmask material is made of an organic material.*

As described above, Chapman and AAPA or Hause render claim 4 obvious. The combination also renders claim 7 obvious. Chapman taught using a BARC hardmask made from "organic" material. Ex. 1004, 6:5-7; Ex. 1002 ¶¶ 129-30.

8. **Claim 8:** *A method of forming circuit structures as claimed in claim 7, wherein the organic material is a bottom anti-reflective coating.*

As described above, Chapman and AAPA or Hause render claim 7 obvious. The combination also renders claim 8 obvious. Chapman described an "organic BARC" hardmask and taught that BARC means "bottom anti-reflective coating." Ex. 1004, 6:5-7, claim 5; Ex. 1002 ¶¶ 131-32.

9. Claim 9: *A method of forming circuit structures as claimed in claim 4, wherein the hardmask layer has a thickness between 50 Å to 500 Å.*

As described above, Chapman and AAPA or Hause render claim 4 obvious. The combination also renders claim 9 obvious. In its fifth embodiment, Chapman taught a BARC hardmask layer having a thickness of 50 nm or 500Å. Ex. 1004, 6:17-19. Chapman taught that the fifth embodiment "could also be used with any of the foregoing preferred embodiment linewidth reduction methods." *Id.*, 6:10-13. Based on that disclosure, Chapman taught combining the method of the fifth embodiment with the linewidth reduction technique disclosed in the fourth embodiment, which requires the isotropic BARC etch described above (at 30). That combination involves using the BARC hardmask layer with a thickness of 500Å as taught in the fifth embodiment and, in order to retain linewidth reduction, performing the steps described in the fifth embodiment after the BARC trimming step of the fourth embodiment.[6] Ex. 1002 ¶¶133-36. Combining these

[6] For the fifth embodiment, Chapman taught optionally etching the photoresist above the BARC layer so that its linewidth was equal to the narrower linewidth of the trimmed BARC layer. Ex. 1004, 6:19-23, Fig. 9a; Ex. 1002 ¶135.

two methods as taught in Chapman disclosed a hardmask thickness within the claimed range.

In addition, and in any event, a skilled person would have used a BARC hardmask of 500Å in Chapman's fourth embodiment, rendering this limitation obvious. Ex. 1002 ¶137. Chapman itself suggests and motivates the combination. A skilled person would have used the known liftoff approach associated with the 500Å BARC hardmask taught in the fifth embodiment to obtain the predictable benefit of removing photoresist or photoresist residue in the process of the fourth embodiment. Ex. 1004, 6:14-16, 6:35-38; Ex. 1002 ¶138; *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 401 (2007) ("a combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results"); *see also id.* at 417 ("If a person of ordinary skill can implement a predictable variation, § 103 likely bars its patentability."). It would have been a simple design choice to use a hardmask with a 500Å thickness, as was known, in the process of the fourth embodiment, including any necessary adjustments to the hardmask etch chemistry. Ex. 1002 ¶¶137-39; *CRFD Research, Inc. v. Matal*, 876 F.3d 1330, 1347 (Fed. Cir. 2017) ("simple design choice" supported obviousness). Chapman itself described that its preferred embodiments and "etch chemistries and conditions" could be "varied." Ex. 1004, 6:52-7:6.

10. Claim 16: *A method of forming circuit structures as claimed in claim 1, wherein the resist mask used in the isotropic etching step is removed prior to the anisotropic etching step of the device layer.*

As described above, Chapman and AAPA or Hause render claim 1 obvious. The combination also renders claim 16 obvious. Following the isotropic etch of the BARC layer (Ex. 1004, 5:49-52), Chapman taught "strip[ping] overlying photoresist 811-812 with an oxygen plasma, and then anisotropically etch[ing]" polysilicon 806—the "device layer" (*id.*, 5:63-65). Ex. 1002 ¶¶166-67.

11. Claim 17: *A method of forming circuit structures as claimed in claim 1, wherein the resist mask used in the isotropic etching step is maintained on top of the hardmask during the anisotropic etching step of the device layer.*

As described above, Chapman and AAPA or Hause render claim 1 obvious. The combination also renders claim 17 obvious. Chapman's fifth embodiment retains the photoresist mask pattern 911 on top of BARC hardmask layer 917 when anisotropically etching polysilicon 906—the "device layer." Ex. 1004, 6:17-28. Annotated Figure 9b below shows the resist (blue), BARC layer (green), and polysilicon layer (yellow) after completing the polysilicon etch. *Id.*, 2:14. The resist was present during the etch of polysilicon and removed later. Ex. 1004, 6:29-34; Ex. 1002 ¶169.

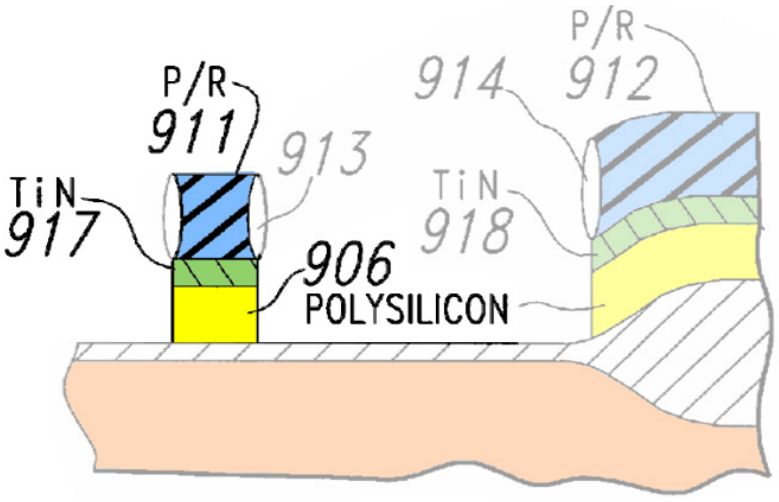


Fig. 9b

As described above (at 34-35), Chapman taught combining its fourth and fifth embodiments to perform the steps of the fifth embodiment after completing the "linewidth reduction" BARC trimming step taught in the fourth embodiment. That combination includes the fifth embodiment's teaching to retain the photoresist mask during the anisotropic etch of polysilicon, as required by claim 17. Ex. 1002 ¶170. Together with the prior art's teachings of UTR layers, the combined process of the fourth and fifth embodiments taught the preamble of claim 1 and limitations 1[a]-1[f] for the same reasons as explained above. As to limitation 1[g], like the fourth embodiment, the fifth embodiment disclosed "anisotropically etch[ing] polysilicon" using BARC layer 911 "as an etch mask." Ex. 1004, 6:24-26. Annotated Figure 9b above shows that the resulting etched polysilicon 906 (yellow) has the same linewidth as BARC layer 917 (green).

Accordingly, the combined method of the fourth and fifth embodiments disclosed limitation 1[g].

In any case, it also would have been obvious to apply Chapman's teachings in the second and fifth embodiments of maintaining the photoresist during the polysilicon etch to the fourth embodiment. Ex. 1002 ¶¶171-72. As Chapman itself reflects, it was known in the prior art to remove resist before an anisotropic etch of polysilicon—or to maintain the resist during that step. Those are the only two options, and Chapman taught both. Ex. 1004, 4:37-45, 5:63-65, 6:17-28. Each approach is predictable and leads to the successful anisotropic etching of polysilicon to obtain sub-lithographic linewidths. *KSR*, 550 U.S. at 421 ("When there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp."). A skilled person would have been motivated to use either technique in the method of the fourth embodiment given that the results were the same for each: anisotropically etched polysilicon having a narrowed linewidth. Ex. 1002 ¶171. Deciding whether to remove or maintain the resist was a simple design choice. *Id.* ¶172; *CRFD Research*, 876 F.3d at 1347. Indeed, the fourth and fifth embodiment overlap: both used a TiN BARC layer. Ex. 1004, 5:23-25, 6:17-19; Ex. 1002 ¶173. Chapman invites varying its embodiments so long as each retains an

intermediate hardmask layer, as is the case for the proposed modification of the fourth embodiment here. Ex. 1004, 6:53-58.

D. Ground 2: Chapman, AAPA or Hause, and Becker or Jeoung or Wong render obvious claims 10-11

As described above (at 23-31), Chapman and Applicant Admitted Prior Art ("AAPA") or Hause render claim 1 obvious. Claims 10 and 11 depend from claim 1 and recite different steps for treating the resist layer to "enhance selectivity to the hardmask layer." Becker, Jeoung, and Wong disclosed the claimed approaches and described why a skilled person would have applied them in the combined method of Chapman and AAPA or Hause.

1. Claim 10: *A method of forming circuit structures as claimed in claim 1, further comprising the step of exposing the resist layer to a UV bake prior to the step of isotropic over-etching so as to enhance selectivity to the hardmask layer.*

Claim 10 adds an extra step to the method of claim 1: exposing the resist layer to a UV bake before the isotropic etch of the hardmask layer to make the etch more selective to the hardmask. The claimed enhanced selectivity means the subsequent isotropic etch wears away the hardmask at a higher rate than the resist. Ex. 1002 ¶141.

Becker taught using a UV bake to stabilize a resist film and make an etching process more selective to an underlying layer. Ex. 1008 at 1126, 1133. Doing so avoids problems relating to "lower process stability, reduced thickness,

and lower thermal stability" of certain resists. *Id.* at 1126. Due to the UV bake stabilization process, one resist showed an etch rate 2.5x slower than an underlying layer. *Id.* at 1128, 1133. Similarly, Jeoung taught UV baking a photoresist to improve its stability. Ex. 1019, 9:36-42. As Becker explained, that stabilization decreased the resist's etch rate.

A skilled person would have used the UV bake technique taught in Becker or Jeoung in conjunction with the combined method of Chapman and AAPA or Hause. Ex. 1002 ¶145. Chapman already taught baking a resist layer before isotropically removing part of a BARC hardmask layer. Ex. 1004, 5:36-37. It would have been obvious to implement Baker's or Jeoung's UV bake as part of that baking step. Implementing that known technique would have improved Chapman's resist layer by stabilizing it and avoiding the other potential issues described in Becker. The UV bake would have increased etch selectivity to the BARC hardmask, as claimed.

2. **Claim 11:** *A method of forming circuit structures as claimed in claim 1, further comprising the step of curing the resist layer by an electron beam prior to the step of isotropic over-etching so as to enhance selectivity to the hardmask layer.*

Claim 11 describes adding a step to claim 1 that differs from the extra step in claim 10, though the effect is the same. Claim 11 recites curing the resist with an electron beam to enhance etch selectivity to the hardmask before the isotropic etch.

That technique was known in the prior art. Becker taught that, like UV baking, applying an electron beam to cure a resist stabilized it. Ex. 1008 at 1126, 1128. The electron beam "improves the thermal stability and enhances the etch resistance of the resist." *Id.* at 1128. As a result, in one example, the etching rate of an underlying layer was between 2.65x and 4x more rapid than a resist treated with an electron beam. *Id.* at 1128, 1133. Likewise, Wong taught curing a resist using an electron beam, noting that "etch rate decreases sharply as e-beam exposure dose increases." Ex. 1020, 9:57-62. The electron beam exposure also made the resist "more thermally stable and mechanically robust." *Id.*, 11:62-66.

Here, too, a skilled person would have applied the electron beam curing described in Becker or Wong before the isotropic hardmask etch in the combined method of Chapman and AAPA or Hause. Ex. 1002 ¶151. Doing so would have provided the benefits described in Becker or Wong of improving Chapman's resist by increasing its stability and etch resistance. The electron beam stabilization also would have avoided problems noted in Becker for resists that have not been stabilized. Ex. 1008 at 1126 ("lower process stability, reduced thickness, and lower thermal stability").

E. Ground 3: Chapman, AAPA or Hause, and Lin or Cirelli render obvious claims 12-15

As described above (at 23-31), Chapman and Applicant Admitted Prior Art ("AAPA") or Hause render claim 1 obvious. Claims 12-15 depend from claim 1

and describe variations of a multilayered hardmask. Lin and Cirelli each taught what is claimed. A skilled person would have incorporated Lin's or Cirelli's teachings into the combined method of Chapman and AAPA or Hause to obtain advantages of the designs described in Lin and Cirelli.

1. Claim 12: *A method of forming circuit structures as claimed in claim 1, wherein the hardmask layer is formed of a multi-layer material.*

Claim 12 narrows claim 1 by requiring that the hardmask layer include multiple layers of material. Lin and Cirelli each taught such a hardmask. Lin's hardmask has a top layer of SiON BARC material, with sublayers for "phase shift cancellation" and "light absorption." Ex. 1009 at 186. The top BARC layer rests on a bottom oxide layer. *Id.* at 187-88, 191. Lin further taught that its multilayered hardmask advantageously reduced the need for "thickness control" of the various layers, which simplified manufacturing. *Id.* at 196. The technique also resulted in "better performance" regarding CD uniformity and process margin. *Id.* Cirelli similarly disclosed a hardmask with a "multilayer ARC stack" on top of an oxide layer. Ex. 1021 at 4231-32. According to Cirelli, this mask absorbed radiation without requiring "tight thickness control" while providing "[e]xcellent imaging and etch performance" together with "superb linewidth control." *Id.* at 4229, 4233. To obtain these known benefits, a skilled person

would have been motivated to use Lin's or Cirelli's multilayered hardmask in the combined method of Chapman and AAPA or Hause. Ex. 1002 ¶156.

Chapman supports and motivates the combination. First, Chapman described using a BARC hardmask (Ex. 1004, 5:22-23), which is the same type of material used in the top layers of Lin's and Cirelli's hardmasks. Second, Chapman contemplated using a hardmask that could act as "an etchstop." *Id.*, 1:61-65, 2:34-39, 6:53-58. Incorporating Lin's or Cirelli's bottom hardmask layer would have achieved that function. Ex. 1002 ¶157. The bottom layer of Lin's and Cirelli's hardmasks is an oxide layer, and as the '097 patent explains, an "oxide film" is an "etchstop layer." Ex. 1001, 4:59-67. An oxide layer has a low etching rate under certain conditions and therefore can protect underlying layers from unwanted etching. Ex. 1002 ¶159. That beneficial function of an oxide layer was known in the art, and adding Lin's or Cirelli's bottom oxide layer would have provided it. Ex. 1002 ¶¶157-59.

2. Claim 13: *A method of forming circuit structures as claimed in claim 12, wherein the multi-layer material consists of a top anti-reflective layer and a bottom etchstop layer.*

As described above, Chapman, AAPA or Hause, and Lin or Cirelli render claim 12 obvious. The combination also renders claim 13 obvious. Ex. 1002 ¶¶160-61. Lin's hardmask includes a top BARC layer and a bottom oxide layer that would have acted as an etchstop. Ex. 1009 at 187-88, 191; Ex. 1001, 4:59-67.

BARC is an anti-reflective coating. Ex. 1004, claim 5. Likewise, Cirelli's top layer was itself a multilayer anti-reflective coating and its bottom layer was an oxide that would have served as an etchstop layer. Ex. 1021 at 4230-31; Ex. 1001, 4:59-67.

3. Claim 14: *A method of forming circuit structures as claimed in claim 13, wherein the top anti-reflective layer is formed of a nitride film.*

As described above, Chapman, AAPA or Hause, and Lin or Cirelli render claim 13 obvious. The combination also renders claim 14 obvious. Ex. 1002 ¶162-63. Lin taught that the top BARC layer was formed of silicon oxynitride or SiON, which is a nitride film. Ex. 1009 at 186. Cirelli disclosed that its top ARC layer could be made from "silicon rich nitrides or oxy-nitrides." Ex. 1021 at 4230.

4. Claim 15: *A method of forming circuit structures as claimed in claim 14, wherein the bottom etchstop layer is formed of an oxide film.*

As described above, Chapman, AAPA or Hause, and Lin or Cirelli render claim 14 obvious. The combination also renders claim 15 obvious. Ex. 1002 ¶¶164-65. Lin and Cirelli each described a bottom oxide layer that would have acted as an etchstop when incorporated into the combined method of Chapman and AAPA or Hause. Ex. 1009 at 187-88, 191; Ex. 1021 at 4231 ("SiO_2"), 4232 ("oxide"); Ex. 1001, 4:59-67.

F. Ground 4: Laaksonen and AAPA or Hause render obvious claims 1-2, 4-9, 12-15 and 17

As described above (at 14-15), like Chapman, Laaksonen taught the hard-mask layer and etching steps claimed in the '097 patent. Indeed, Laaksonen taught all limitations of claim 1, except the UTR layer. As reflected in Applicant Admitted Prior Art ("AAPA") or Hause, UTR layers were known in the prior art. Further, a skilled person would have enhanced Laaksonen's process by incorporating a UTR to obtain known benefits. In combination, Laaksonen and AAPA or Hause render claims 1-2, 4-9, 12-15, and 17 obvious.

1. Claim 1:

a. 1[pre]: *A method of forming circuit structures having linewidths which are smaller than what is achievable by conventional UV lithographic techniques on ultra-thin resist layers, said method comprising the steps of:*

To the extent the preamble is limiting, Laaksonen and AAPA or Hause render it obvious. Laaksonen "generally relates to transistor formation" and described a "process for forming a polysilicon line having linewidths below the lithography tool limits." Ex. 1006, 1:9-11, 1:52-53. That process results in "lines having a minimum dimension less than the practical resolution limits of the lithography tool (e.g., less than 0.18 μm for deep UV lithography)." *Id.*, 2:1-5. To obtain such linewidths, the process used a photoresist layer. *Id.*, 2:67-3:1.

The preamble of claim 1 requires a UTR layer. As described above (at 24-25), the '097 patent discloses UTR layers as AAPA and establishes that UTR

layers and the benefits they provide were general knowledge to skilled artisans at the time of the alleged invention. For the same reasons described above regarding Chapman's method, a skilled person would have incorporated a UTR layer into Laaksonen's process based on the general knowledge reflected in the disclosures of the '097 patent. Ex. 1002 ¶177.

Furthermore, a skilled person also would have incorporated the UTR layer disclosed in Hause into Laaksonen's process. Ex. 1002 ¶¶179-81. Hause disclosed a UTR layer having a thickness of 2000Å. Ex. 1007, 4:14-17. Laaksonen described a resist with a thickness of 7700Å (Ex. 1006, 3:8-10) but also suggested that "many other thickness variations are possible" (*id.*, 3:12-15). Hause disclosed that using a photoresist with a "thickness on the order of 8000 … angstroms," such as the one taught in Laaksonen, "may be too large to accurately replicate the image pattern." Ex. 1007, 2:22-25. By contrast, Hause's UTR layer "replicates the first image pattern with a high degree of accuracy" (*id.*, 4:25-27)—"more accurately than thicker photoresist layers" (*id.*, 2:40-44) like the one Laaksonen taught. Because implementing Hause's UTR layer as part of Laaksonen's process would have improved patterning accuracy, a skilled person would have pursued the combination. Ex. 1002 ¶¶181-82. Further, known improvements in process control would have provided another reason for a skilled

person to use a UTR layer in Laaksonen's process. Ex. 1024 at 4251; Ex. 1002 ¶178.

b. 1[a]: *providing a semiconductor wafer stack formed of a substrate and a device layer above the substrate;*

Laaksonen disclosed a semiconductor device having multiple layers. Ex. 1006, 2:54-3:3. Annotated Figure 2 below shows photoresist layer 32 (blue), BARC layer 30 (green), polysilicon layer 20 (yellow), and semiconductor body 10 (orange). Polysilicon layer 20—the "device layer"—is above semiconductor body 10—the "substrate." Ex. 1002 ¶183.

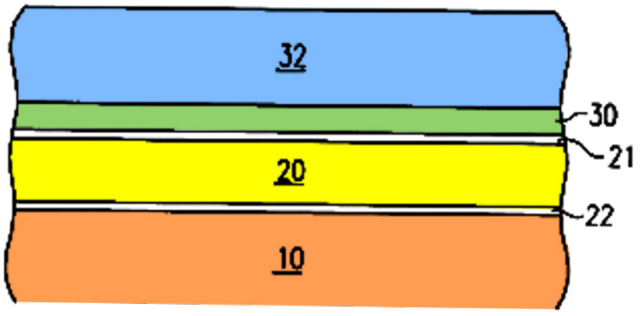


FIG. 2

The '097 patent makes clear that the "device layer" is a "gate conductive layer" (Ex. 1001, 3:63-65) and can be made from silicon (claim 2). Laaksonen's polysilicon layer 20 is a "device layer" because it has the same features. It is used for gate formation and made from polycrystalline silicon. Ex. 1006, 5:3-4. As described above (at 27-28), under Ocean's interpretation of this limitation, gate dielectric 22 does not alter that polysilicon layer 20 is "above" semiconductor body 10.

c. 1[b]: *depositing a hardmask layer over the device layer;*

As shown in annotated Figure 2 above, Laaksonen taught that BARC layer 30 (green) "is deposited over polysilicon layer 20" (yellow)—the "device layer." Ex. 1006, 2:64-65. BARC layer 30 functions as an etching mask: its width after etching determines the eventual width of lines etched from polysilicon. *Id.*, 4:17-26; *see also id.*, 4:34-35 ("Overall linewidth reduction is controlled by the BARC etch."); Ex. 1002 ¶187. The '097 patent identifies BARC as one example of a hardmask layer. Ex. 1001, 4:4-8.

d. 1[c]: *depositing an ultra-thin resist layer over the hard-mask layer;*

Annotated Figure 2 above shows that Laaksonen's layer stack includes photoresist 32 "deposited over" BARC layer 30. Ex. 1006, 2:67-3:1; Ex. 1002 ¶189. As described above (at 45-47), it would have been obvious to incorporate a UTR layer into Laaksonen's process.

e. 1[d]: *forming a resist mask having an initial linewidth;*

Laaksonen taught that "pattern 40 is created from the resist layer 32." Ex. 1006, 3:24-25. Resist pattern 40 has an initial width of "Lp." *Id.*, 3:26-28, Fig. 1. The pattern is used as a mask to etch the underlying BARC layer. *Id.*, 3:30-33, Fig. 4; Ex. 1002 ¶191. Annotated Figure 3 below shows resist pattern 40 (blue).

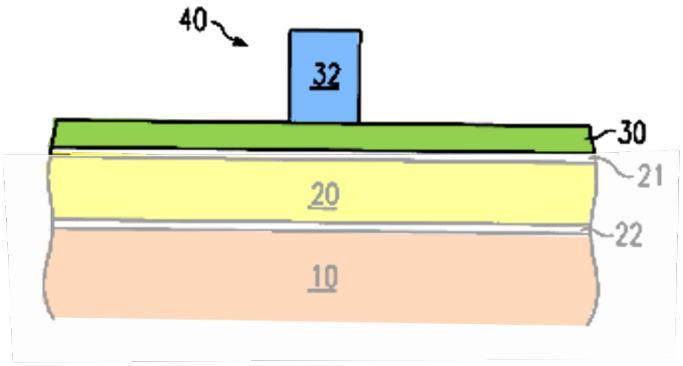


FIG. 3

f. 1[e]: *anisotropically etching exposed portions of the hardmask layer;*

Laaksonen taught etching BARC layer 30 (green) with "a mainly vertical component" to remove exposed portions of that layer not covered by resist pattern 40 (blue), as shown in annotated Figure 4 below. Ex. 1006, 3:30-33; *see also id.*, 3:34-66 ("BARC clears from the surface"); Ex. 1002 ¶¶ 192-93. This is the same primarily unidirectional (vertical) anisotropic etch of exposed portions of a hardmask as taught in Chapman (Ex. 1004, 5:40-41, Fig. 8c) and described in the '097 patent (Ex. 1001, 4:67-5:5).

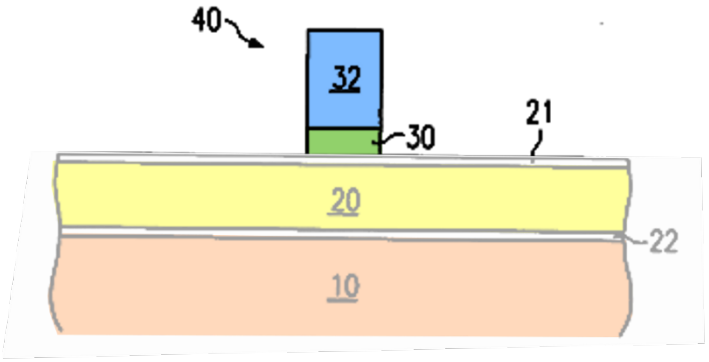


FIG. 4

g. 1[f]: *isotropically etching subsequently the hardmask layer underneath the resist mask to form a hardmask having a final linewidth which is narrower than the initial line width of the resist mask and corresponds to a desired structure linewidth; and*

After the anisotropic BARC etch, an "overetch" is performed that includes a "horizontal component" that "reduces the lateral dimension of both the resist and BARC." Ex. 1006, 3:33-38. This omnidirectional etching step results in reduced width pattern 50 for resist 32 (blue) and a hardmask underneath it—BARC 30 (green), as shown in annotated Figure 5 below. *Id.*, 3:38-66. Laaksonen's overetch is isotropic. Ex. 1002 ¶¶ 194-96. First, Rogers—an earlier Texas Instrument's patent with nearly identical figures and disclosures as Laaksonen—explicitly described the same overetching step under the same circumstances as "an isotropic etch." Ex. 1005, 1:45-49; *compare* Ex. 1006, 1:61-64. Second, Laaksonen's teachings mirror the '097 patent's disclosures of an omnidirectional isotropic etch. The '097 patent describes an "isotropic etch" as "reduc[ing] the lateral dimension" of the hardmask (Ex. 1001, 4:67-5:5), which is the same language used in Laaksonen to describe its overetch step.

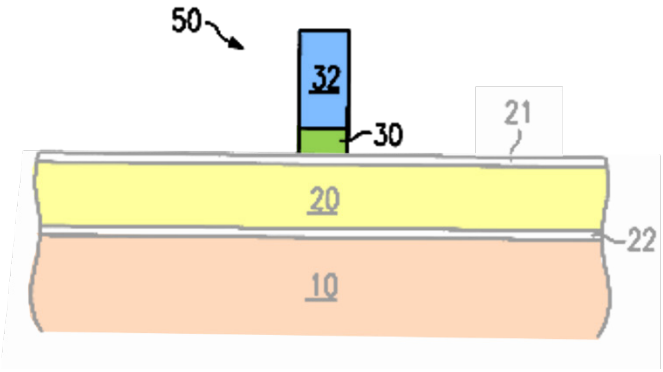


FIG. 5

Annotated Figure 1 below depicts the difference between the initial linewidth of resist pattern 40 and the final linewidth of BARC layer 30. At first, resist pattern 40 (blue line) has a linewidth "Lp." Ex. 1006, 2:38-40. After the isotropic overetch, BARC layer 30 (green) has a much narrower linewidth "Lrw." *Id.*, 2:45-48. "Lrw is the desired width of the polysilicon line." *Id.*, 2:49-51; Ex. 1002 ¶197-98.

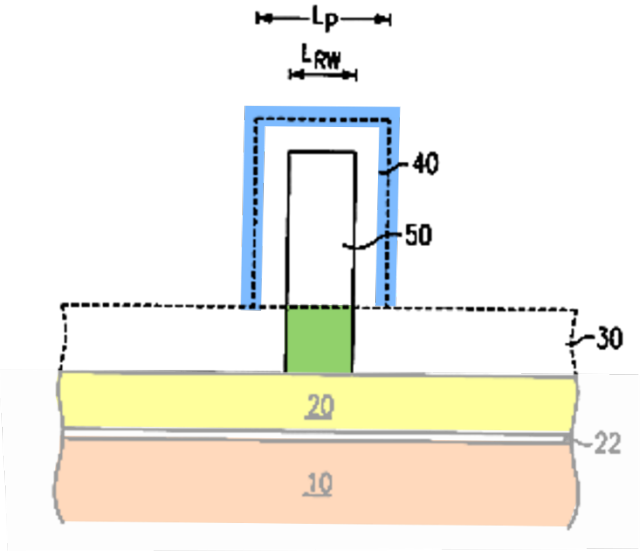


FIG. 1

h. 1[g]: *anisotropically etching the device layer as defined by the hardmask to form a structure having a width substantially equal to the final linewidth of the hardmask.*

Upon completion of the isotropic BARC overetch, Laaksonen taught etching polysilicon layer 20—the "device layer"—using reduced width 50 of BARC layer 30. Ex. 1006, 4:18-19. As shown in annotated Figure 6 below, the etch removes any polysilicon not covered by BARC layer 30 (green), leaving polysilicon line 36 (yellow). *Id.*, 4:21-25.

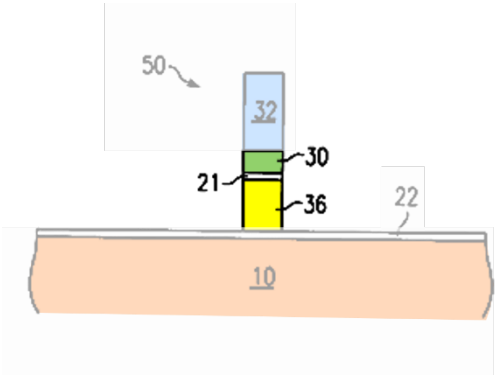


FIG. 6

Laaksonen taught this etch is anisotropic (mainly vertical), not isotropic (omnidirectional). *Id.*, 4:33-35 ("The polysilicon etch itself does not significantly contribute to linewidth reduction. Overall linewidth reduction is controlled by the BARC etch."); Ex. 1002 ¶¶199-201. Further, Laaksonen's teachings for this final anisotropic etch track the description in the '097 patent. The patent describes the corresponding etch step as "anisotropic." Ex. 1001, 4:34-39, Fig. 4f.

In addition, polysilicon line 36 has the same reduced width 50 as BARC layer 30. Ex. 1006, 2:46-51, Fig. 1. In other words, as claimed, polysilicon layer 20—the "device layer"—is etched to form line 36—a "structure"—having a final linewidth substantially equal to BARC layer 30—the "hardmask."

2. Claim 2: *A method of forming circuit structures as claimed in claim 1, wherein the device layer is formed of silicon.*

As described above, Laaksonen and AAPA or Hause render claim 1 obvious. The combination also renders claim 2 obvious. Laaksonen's "device layer" is polysilicon layer 20. Ex. 1006, 2:56-57. Polysilicon is a polycrystalline form of silicon. Ex. 1002 ¶¶202-03.

3. Claim 4: *A method of forming circuit structures as claimed in claim 1, wherein the ultra-thin resist layer has a thickness of less than 2500 Å.*

As described above, Laaksonen and AAPA or Hause render claim 1 obvious. As further described above (at 45-47), the combination would have included a UTR layer with a thickness under 2500Å.

4. Claim 5: *A method of forming circuit structures as claimed in claim 4, wherein the hardmask is made of an inorganic material.*

As described above, Laaksonen and AAPA or Hause render claim 4 obvious. The combination also renders claim 5 obvious. Ex. 1002 ¶¶210-11. Laaksonen taught that BARC layer 30—a "hardmask layer"—could be made from an "inorganic" material. Ex. 1006, 2:65-67.

5. **Claim 6:** *A method of forming circuit structures as claimed in claim 5, wherein the inorganic material is one of silicon dioxide, silicon nitride, silicon oxynitride, and titanium nitride.*

As described above, Laaksonen and AAPA or Hause render claim 5 obvious. The combination also renders claim 6 obvious. Ex. 1002 ¶¶212-13. Laaksonen provided "SiO_xN_y" or silicon oxynitride as an example of an inorganic material to use for a BARC hardmask. Ex. 1006, 5:11-13.

6. **Claim 7:** *A method of forming circuit structures as claimed in claim 4, wherein the hardmask material is made of an organic material.*

As described above, Laaksonen and AAPA or Hause render claim 4 obvious. The combination also renders claim 7 obvious. Ex. 1002 ¶214. Laaksonen taught that BARC layer 30—a "hardmask layer"—could be made from an "organic" material. Ex. 1006, 2:65-67. Organic BARC materials were well known in the prior art. Ex. 1025 at 207-09; Ex. 1002 ¶215.

7. **Claim 8:** *A method of forming circuit structures as claimed in claim 7, wherein the organic material is a bottom anti-reflective coating.*

As described above, Laaksonen and AAPA or Hause render claim 7 obvious. The combination also renders claim 8 obvious. Ex. 1002 ¶¶216-17. As described above (at 48), Laaksonen taught using BARC as a hardmask. Laaksonen also defined "BARC" as "bottom anti-reflective coating." Ex. 1006, 1:34-36.

8. Claim 9: *A method of forming circuit structures as claimed in claim 4, wherein the hardmask layer has a thickness between 50 Å to 500 Å.*

As described above, Laaksonen and AAPA or Hause render claim 4 obvious. The combination also renders claim 9 obvious. In an alternative embodiment, Laaksonen taught a BARC hardmask layer with a thickness of 300Å, which is within the claimed range. Ex. 1006, 5:11-14.

A skilled person would have incorporated the disclosed 300Å BARC layer into the method of Laaksonen's primary embodiment as described in Figures 1-6 and the accompanying text. Ex. 1002 ¶¶219-20. Laaksonen suggested the combination. The description of the primary embodiment states that many "thickness variations are possible," noting that the thicknesses provided for the BARC and resist layers are "an example only." Ex. 1006, 3:8-15. Laaksonen also indicated that "[v]arious … combinations of the illustrative embodiments … will be apparent" to skilled persons. *Id.*, 5:27-30.

In addition, the 300Å BARC layer in Laaksonen's alternative embodiment is made from an inorganic material, silicon oxynitride. Ex. 1006, 5:11-12. The primary embodiment taught that the BARC layer could be made from an inorganic material. *Id.*, 5:65-67. Silicon oxynitride was beneficial because it allowed for a "significantly thinner" BARC layer. *Id.*, 5:13-14.

The various BARC materials and thicknesses taught in Laaksonen, as well as the related etch chemistries, were routine design choices based on known techniques and outcomes. Ex. 1002 ¶222; *CRFD Research*, 876 F.3d at 1347. Regardless of which BARC thickness was used, Laaksonen's two embodiments achieved the same result: reducing linewidths by etching a BARC layer. Ex. 1006, 4:30-37, 5:19-20. Further, the '465 application to which Laaksonen claims priority expressly taught isotropically etching a 300Å BARC layer, just as would have been done when modifying Laaksonen's primary embodiment to include such a layer. Ex. 1012, 10:14-15. Similarly, as described above (at 34-35) regarding claim 9 and Chapman, Chapman disclosed trimming a hardmask (as taught in Laaksonen's primary embodiment) when the hardmask had a thickness (500Å) on the same order as the BARC layer in Laaksonen's alternative embodiment (300Å).

1. Claim 12: *A method of forming circuit structures as claimed in claim 1, wherein the hardmask layer is formed of a multi-layer material.*

As described above, Laaksonen and AAPA or Hause render claim 1 obvious. The combination also renders claim 12 obvious. Laaksonen taught that native oxide layer 21 can form over polysilicon layer 20. Ex. 1006, 2:61-63, 4:4-5. In that case, native oxide layer 21 and BARC layer 30 form a multilayered hardmask. Because the native oxide did not always form, a skilled person would

have deposited an oxide layer between the BARC and polysilicon layers to protect the polysilicon from unwanted etching. Ex. 1002 ¶¶236-38. Laaksonen taught that benefit of an oxide layer and disclosed oxide layer deposition. Ex. 1006, 2:61-63, 4:4-5. As shown in Figure 6 below, like BARC layer 30 (green), native oxide layer 21 (also green) is part of the mask for etching polysilicon layer 20 to obtain polysilicon line 36 (yellow). *Id.*, Fig. 6. If an alternative deposited oxide layer were used, it would have appeared between BARC and polysilicon layers and also served as an etch mask.

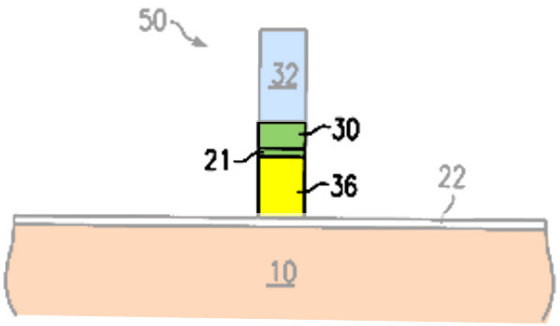


FIG. 6

2. Claim 13: *A method of forming circuit structures as claimed in claim 12, wherein the multi-layer material consists of a top anti-reflective layer and a bottom etchstop layer.*

As described above, Laaksonen and AAPA or Hause render claim 12 obvious. The combination also renders claim 13 obvious. The multilayered hardmask described above for claim 12, as shown in Figure 6, includes the claimed layers. The top layer is BARC layer 30, which is an "anti-reflective coating." Ex. 1006, 1:34-36. The bottom layer is native oxide layer 21, which

protects the polysilicon layer from being etched during BARC etching. *Id.*, 4:4-5 ("Thus, thin native oxide 21 that normally forms over the polysilicon layer 20 protects the polysilicon."). In other words, native oxide layer 21 serves as an "etchstop" layer for the underlying polysilicon. Ex. 1002 ¶¶239-41. An alternative deposited oxide would have functioned in the same way. *Id.* ¶240. Notably, the '097 patent describes an "oxide film" as an "etchstop layer." Ex. 1001, 4:59-67.

3. Claim 14: *A method of forming circuit structures as claimed in claim 13, wherein the top anti-reflective layer is formed of a nitride film.*

As described above, Laaksonen and AAPA or Hause render claim 13 obvious. The combination also renders claim 14 obvious. Ex. 1002 ¶¶242-43. Laaksonen disclosed that the top anti-reflective layer could be made from silicon oxynitride ("SiO_xN_y"), which is a nitride film. Ex. 1006, 5:11-12.

4. Claim 15: *A method of forming circuit structures as claimed in claim 14, wherein the bottom etchstop layer is formed of an oxide film.*

As described above, Laaksonen and AAPA or Hause render claim 14 obvious. The combination also renders claim 15 obvious. Ex. 1002 ¶244. Laaksonen taught a bottom etchstop layer made from oxide: native oxide layer 21. Ex. 1006, 2:61-63. It also would have been obvious to deposit an oxide layer. Ex. 1002 ¶245.

5. Claim 17: *A method of forming circuit structures as claimed in claim 1, wherein the resist mask used in the isotropic etching step is maintained on top of the hardmask during the anisotropic etching step of the device layer.*

As described above, Laaksonen and AAPA or Hause render claim 1 obvious. The combination also renders claim 17 obvious. Ex. 1002 ¶¶248-50. Claim 17 requires maintaining the resist mask used during isotropic etching of a hardmask throughout the final anisotropic etch step of claim 1. Annotated Figure 5 below shows that resist 32—the "resist mask"—remains after the isotropic etch that reduces the linewidth of the resist (blue) and underlying BARC hardmask layer 30 (green). Ex. 1006, 3:33-66.

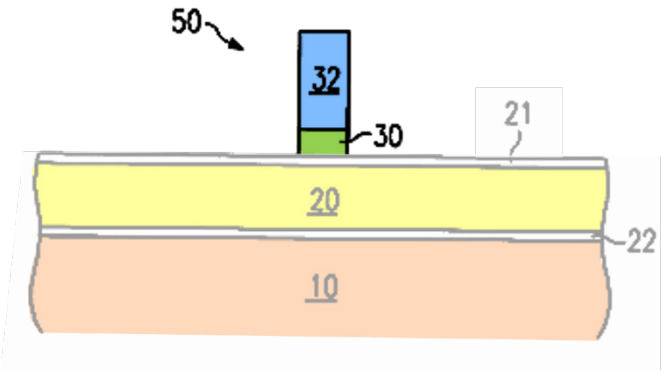


FIG. 5

Annotated Figure 6 below shows that resist 32 (blue) is maintained on top of BARC hardmask layer 30 (green) during the anisotropic etch of polysilicon layer 20 that results in polysilicon line 36 (yellow). *Id.*, 4:18-26. The resist is still evident after the etch.

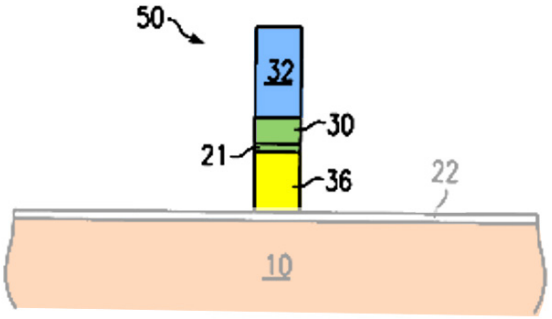


FIG. 6

G. Ground 5: Laaksonen, AAPA or Hause, and Chapman render obvious claims 3 and 16

As described above (at 45-53), Laaksonen and Applicant Admitted Prior Art ("AAPA") or Hause render claims 1 and 2 obvious. Claims 3 and 16 depend from claims 1 and 2, and recite a layer of silicon having a thickness of 500Å-5000Å (claim 3) and removing the resist mask used in isotropic etching before the final anisotropic etch of claim 1 (claim 16). Chapman disclosed the claimed features, and a skilled person would have applied Chapman's teachings in the combined process of Laaksonen and AAPA or Hause.

1. Claim 3: *A method of forming circuit structures as claimed in claim 2, wherein the silicon has a thickness between 500 Å to 5000 Å.*

As described above, Laaksonen and AAPA or Hause render claims 1 and 2 obvious. As also described above (at 32), Chapman taught a polysilicon layer having a thickness of 4000Å. A skilled person would have used a polysilicon layer having that thickness in the combined process of Laaksonen and AAPA or Hause. Ex. 1002 ¶206. Like Chapman, Laaksonen disclosed a polysilicon layer

that is etched after trimming a BARC hardmask. Ex. 1004, 5:49-62; Ex. 1006, 3:30-37, 4:18-19. But Laaksonen did not disclose any specific thickness for the polysilicon layer. Ex. 1006, 2:56-57. Chapman identifies a thickness of polysilicon that is conducive to anisotropic etching after a hardmask trim step to produce a linewidth narrower than allowed by available lithographic techniques. Ex. 1004, 6:2-4. Laaksonen sought to achieve the same outcome. Ex. 1006, 1:52-53. Using the polysilicon layer thickness taught in Chapman would have been obvious because doing so merely applied a known thickness of polysilicon to yield a predicable result—reduced gate linewidth. *KSR*, 550 U.S. at 401. That result was also a major objective described in Laaksonen, and the use of Chapman's teachings would have helped achieve it.

2. Claim 16: *A method of forming circuit structures as claimed in claim 1, wherein the resist mask used in the isotropic etching step is removed prior to the anisotropic etching step of the device layer.*

As described above, Laaksonen and AAPA or Hause render claim 1 obvious. As further described above (at 36), Chapman taught removing a resist mask used during isotropic etching of a hardmask before anisotropically etching a polysilicon layer. A skilled person would have applied Chapman's teachings of removing the resist mask in the combined process of Laaksonen and AAPA or Hause. Ex. 1002 ¶¶246-47. As Chapman demonstrates, it was known in the prior art to remove resist before an anisotropic etch of polysilicon rather than

maintaining it, as taught in Laaksonen. Laaksonen taught that "other suitable polysilicon etch processes will be apparent to those of ordinary skill in the art." Ex. 1006, 4:25-27.

A skilled person would have known that there were just two options for dealing with photoresist after the isotropic hardmask trim step taught in Chapman and Laaksonen (Ex. 1004, 5:49-62; Ex. 1006, 3:30-37) and before the polysilicon etch: maintain it or remove it. Ex. 1002 ¶228. As Chapman and Laaksonen disclosed, either approach resulted in the same predictable result of successfully etching a polysilicon layer to obtain sub-lithographic linewidths. Both techniques are therefore obvious. *KSR*, 550 U.S. at 401. And both approaches were within the grasp of a skilled person such that altering Laaksonen's process to remove the resist would have been a simple design choice. Ex. 1002 ¶229; *KSR*, 550 U.S. at 421; *CRFD Research*, 876 F.3d at 1347. A skilled person would have applied Chapman's teachings of a successful polysilicon etch based on photoresist removal and a known inorganic hardmask (TiN) to Laaksonen's primary embodiment—especially given that Laaksonen taught using an inorganic hardmask (Ex. 1006, 2:65-3:1). Ex. 1002 ¶229.

H. Ground 6: Laaksonen, AAPA or Hause, Chapman, and Becker or Jeoung or Wong render obvious claims 10-11

As described above (at 45-53), Laaksonen and Applicant Admitted Prior Art ("AAPA") or Hause render claim 1 obvious. Claims 10 and 11 depend from

claim 1 and describe UV baking (claim 10) and electron beam curing (claim 11) a resist layer to "enhance selectivity to the hardmask layer." Becker, Jeoung, and Wong taught those techniques, as well as the advantages they provide. Because of those advantages, a skilled person would have incorporated Becker's, Jeoung's, or Wong's techniques into the combined process of Laaksonen and AAPA or Hause. It also would have been obvious to remove the resist mask after the isotropic hardmask etch and before the anisotropic device layer etch, as disclosed in Chapman.

1. **Claim 10:** *A method of forming circuit structures as claimed in claim 1, further comprising the step of exposing the resist layer to a UV bake prior to the step of isotropic over-etching so as to enhance selectivity to the hardmask layer.*

The claimed UV baking of a photoresist before isotropically etching a hardmask makes the etch more selective to the hardmask layer, meaning the hardmask will be consumed at a higher rate than the resist during the etch. Ex. 1002 ¶225.

Becker disclosed a UV baking process for stabilizing a resist film and making an etch more selective for a layer under the resist. Ex. 1008 at 1126, 1133. The UV bake resolved issues with the resist, including "lower process stability, reduced thickness, and lower thermal stability." *Id.* at 1126. And after UV baking, a resist had a slower etch rate than the layer underneath it. *Id.* at 1128, 1133. Jeoung also disclosed a UV bake process that resulted in a more

stable resist. Ex. 1019, 9:36-42. Becker explained that an increase in resist stability corresponds to a lower resist etching rate.

A skilled person would have used the UV bake approach disclosed in Becker or Jeoung in the combined process of Laaksonen and AAPA or Hause. Ex. 1002 ¶226. As described above (at 48-51), Laaksonen taught using resist as a mask when anisotropically and isotropically etching a BARC hardmask layer. And Becker disclosed that stabilizing the resist through, for example, UV baking "improve[s] the performance of the resist" when it was "used as a mask." Ex. 1008 at 1127. Jeoung also taught an improvement in resist stability. Ex. 1019, 9:36-42. To stabilize and improve the resist in the combined process of Laaksonen and AAPA or Hause, a skilled person would have included a UV baking step before the anisotropic and isotropic etch steps for the BARC hardmask. Ex. 1002 ¶226.

It also would have been obvious to apply Chapman's teaching of removing a resist mask before etching polysilicon lines using a BARC hardmask. Ex. 1002 ¶227. After an isotropic etch of a BARC layer, it was possible either to leave an overlying resist mask used for that etch or to remove it. There are no other possibilities. Chapman disclosed removing the resist mask and achieving sub-lithographic linewidths for polysilicon structures after that removal. Ex. 1004, 5:49-62. Applying Chapman's technique would have accomplished that same

predictable outcome in the combined process of Laaksonen, AAPA or Hause, and Becker or Jeoung, rendering the approach obvious. *KSR*, 550 U.S. at 401.

2. Claim 11: *A method of forming circuit structures as claimed in claim 1, further comprising the step of curing the resist layer by an electron beam prior to the step of isotropic over-etching so as to enhance selectivity to the hardmask layer.*

Like claim 10, claim 11 recites treating resist to enhance etch selectivity to an underlying hardmask. Claim 11 describes using an electron beam to cure the resist and achieve the desired etch selectivity.

Becker and Wong each disclosed the claimed technique. Becker described processing a resist using an electron beam, which stabilized the resist. Ex. 1008 at 1126, 1128. Becker further explained that the electron beam treatment "improves the thermal stability and enhances the etch resistance of the resist." *Id.* at 1128. According to the experimental results reported in Becker, a treated resist etched at a rate 2.65x and 4x slower than an underlying layer. *Id.* at 1128, 1133. Wong similarly disclosed that electron beam exposure made the resist "more thermally stable and mechanically robust." Ex. 1020, 11:62-66. The exposure "sharply" reduced the etching rate for treated resist. *Id.*, 9:57-62, 11:17-30, Fig. 1.

In the combined process of Laaksonen and AAPA or Hause, a skilled person would have applied Becker's or Wong's electron beam processing to the resist before the isotropic etch of the BARC hardmask layer. Ex. 1002 ¶234. Electron beam processing would have provided the benefits described in Becker

and Wong, including thermal stabilization and etch resistance (Ex. 1008 at 1126-27; Ex. 1020, 9:57-62, 11:62-66) to improve the overall performance of the resist, which acts as a mask when etching the BARC hardmask layer described in Laaksonen. Further, as described above for claim 10, it would have been obvious to remove the resist mask before using the BARC hardmask to etch polysilicon in the combined process of Laaksonen, AAPA or Hause, Becker or Wong, and Chapman.

VII. ST'S PRIOR ART AND ARGUMENTS ARE NEW TO THE PATENT OFFICE

This Petition relies on prior art and arguments not presented to the Patent Office during prosecution of the '097 patent. Accordingly, the criteria of 35 U.S.C. § 325(d) do not apply. Under the two-step framework for evaluating those criteria, the Board first considers whether the same or substantially the same art or arguments were presented previously to the PTO. *Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GMBH*, IPR2019-01469, Paper 6, at 8 (PTAB Feb. 13, 2020) (precedential). The Board proceeds to step two—whether the Patent Office erred—only if the first condition is satisfied. *Id*. Here, the inquiry ends at step one.

The primary references cited in this Petition—Chapman and Laaksonen—were not presented to the Patent Office during prosecution of the '097 patent. The same is true for Lin, Cirelli, Becker, Jeoung, and Wong. Accordingly, the Patent

Office has never considered the teachings of those references or their effect on the patentability of the '097 patent's claims. Because of this new art, the combinations and arguments described in the Petition are unique and not cumulative of the prior art and arguments considered by the Patent Office during prosecution. For example, the examiner allowed the claims over the prior art of record during prosecution because those references failed to teach "three etching steps including an anisotropic etch of the hardmask layer, an isotropic etch of the hardmask, and an anisotropic etch of the underlying layers." Ex. 1003 at 71. As described above (at 11-15), Chapman and Laaksonen each taught the three claimed etching steps that were missing from the art considered during prosecution. Accordingly, the prior art combinations based on Chapman and Laaksonen described in this Petition differ substantially from the references and combinations considered during prosecution.[7]

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[7] Even though Hause was identified as prior art during prosecution, the examiner did not rely on it to reject any claims. That "weighs strongly" against applying § 325(d) to deny institution. *Solaredge Techs. Ltd. v. SMA Solar Tech. AG*, IPR2020-00021, Paper 8 at 11-12 (PTAB Apr. 10, 2020).

VIII. CO-PENDING DISTRICT COURT LITIGATION IN TEXAS SHOULD NOT PRECLUDE INSTITUTION

Although there is concurrent district court litigation in the Western District of Texas involving the '097 patent, the weight of the factors described in *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 5-6 (PTAB Mar. 20, 2020) (precedential) favors institution of review based on this Petition.

A. The potential for a stay of the district court case urges against denial (factor 1)

After any institution of review based on this Petition, ST intends to seek a stay of the co-pending district court proceedings. Under such circumstances, factor 1 is neutral because any decision by the district court to stay the case would issue after institution and be based on "a variety of circumstances and facts beyond [the Board's] control and to which the Board is not privy." *See Sand Revolution II, LLC v. Cont'l Intermodal Grp. Trucking, LLC*, IPR2019-01393, Paper 24 at 7 (PTAB June 16, 2020) (informative).

B. Uncertainty over the trial date in the Texas case favors institution (factor 2)

The district court recently entered a Scheduling Order identifying December 7, 2022 as the target trial date, although the court noted it "expects to set th[e] date at the conclusion of the *Markman* hearing." Ex. 1015 at 4. Based on the standard 18-month IPR schedule, a final written decision in this proceeding

would likely issue in or around February 2023, within a couple of months of the court's initial target date for trial.

The close proximity between the district court's target trial date and the Board's final written decision date favors institution, or is neutral, because the district court's trial date is subject to considerable uncertainty. *Sand Revolution*, IPR2019-01393, Paper 24 at 9-10 (uncertainty of trial date weighed in favor of institution) (informative); *Micron Tech., Inc. v. Godo Kaisha IP Bridge 1*, IPR2020-01008, Paper 10 at 14 (PTAB Dec. 7, 2020) ("due to the uncertainty as to this trial date, this factor is, at most, neutral to whether we should exercise our discretion to deny the Petition").

Despite the district court's aspirational target date, trial probably will not begin on December 7, 2022 and may be postponed until after the Board issues a final written decision in any instituted IPR proceeding. Delays could result from (i) the continued impact of and uncertainty created by the COVID-19 pandemic, (ii) the crowded docket of the court in the Western District of Texas where the co-pending litigation is set—that docket currently includes over 857 pending patent cases (Ex. 1017), and (iii) the tendency for trial dates in the Western District of Texas to slip from the court's initial target dates—Ex. 1016 at 3 ("In the WDTX, 70% of trial dates initially relied upon by the PTAB to deny petitions have slid.").

Furthermore, Ocean has asserted numerous patents against seven different defendants (including ST) in separate but parallel cases in the Western District of Texas:

- *Ocean Semiconductor LLC v. MediaTek Inc.*, No. 6:20-cv-01210 (W.D. Tex.);
- *Ocean Semiconductor LLC v. NVIDIA Corp.*, No. 6:20-cv-01211 (W.D. Tex.);
- *Ocean Semiconductor LLC v. NXP Semiconductors NV*, No. 6:20-cv-01212 (W.D. Tex.)
- *Ocean Semiconductor LLC v. Renesas Elecs. Corp.*, No. 6:20-cv-01213 (W.D. Tex.)
- *Ocean Semiconductor LLC v. Silicon Laboratories Inc.*, No. 6:20-cv-01214 (W.D. Tex.)
- *Ocean Semiconductor LLC v. STMicroelectronics Inc.*, No. 6:20-cv-01215 (W.D. Tex.); and
- *Ocean Semiconductor LLC v. Western Digital Technologies, Inc.*, No. 6:20-cv-01216 (W.D. Tex.).

All these cases have the same target trial date: December 7, 2022. Of course, the district court cannot try more than one case at a time. As indicated by its case number, the lawsuit against ST was the second-to-last filed by Ocean, which

suggests that trials for other defendants in earlier-filed cases will likely proceed first, delaying any potential trial in the case against ST.

In contrast to the potential delays to the district court's schedule, the Board's schedule is unlikely to shift. Barring exceptional circumstances, the Board must issue its final written decision within the one-year statutory deadline described in 35 U.S.C. § 316(a)(11). *Sand Revolution*, IPR2019-01393, Paper 24 at 9. Further, the Board has remained fully operational despite the challenges presented by COVID-19. *Id.* Given the circumstances, the Board may well issue a final written decision before the beginning of any trial in the ST case in Texas.

Factor 2 also favors institution because ST diligently filed this Petition several months before its statutory deadline for doing so. *See, e.g.*, *Apple Inc. v. Seven Networks, LLC*, IPR2020-00156, Paper 10 at 9 & n.8 (PTAB June 15, 2020).

C. Investment in the parallel district court proceeding is minimal and ST was diligent in filing this Petition (factor 3)

Factor 3 favors institution. The co-pending district court case is still in an early phase. The court has not addressed the merits of the case. All significant stages of litigation—including discovery, claim construction, summary judgment, and trial—remain in the future. The target trial date is over 15 months away and will likely be delayed. In addition, after receiving any institution decision, ST intends to move for a stay in the district court to minimize investment by the court

and the parties by postponing as much of the litigation as possible. Moreover, ST was diligent in filing this Petition over four months before its statutory bar date of January 5, 2022 and less than two months after receiving Ocean's infringement contentions relating to the '097 patent in early July 2021. *See Seven Networks*, IPR2020-00156, Paper 10 at 11 (filing petition four months before § 315(b) bar date shows diligence).

D. The Petition raises unique issues, which favors institution (factor 4)

This Petition addresses claims that the district court will never address. Ocean has identified claims 1-14 and 17 as asserted claims in the district court litigation (Ex. 1011 at 3-4), while ST challenges all 17 claims of the '097 patent in this proceeding. ST has a substantial interest in resolving the patentability of all challenged claims, which the Board will be in a unique position to assess. For example, addressing all 17 claims at once would potentially prevent Ocean from initiating a second, separate round of costly litigation against ST based on claims 15 and 16. The difference in scope between the claims at issue in the district court case and this Petition favors institution. *See Seven Networks*, IPR2020-00156, Paper 10 at 21.

Moreover, ST expects its invalidity positions in the district court case will diverge from the grounds of unpatentability described in this Petition. In any event, ST reserves the right to enter a stipulation that it will not pursue invalidity

in the district court based on the same grounds asserted in this Petition, should the Board deem one necessary. Such a stipulation would mitigate concerns about duplicative efforts in the district court case and this IPR proceeding. *See Sand Revolution*, IPR2019-01393, Paper 24 at 12.

E. The parties overlap (factor 5)

The district court case and the IPR proceeding involve the same parties.

F. The merits of ST's challenge support institution (factor 6)

"[I]f the merits of a ground raised in the petition seem particularly strong on the preliminary record … the institution of a trial may serve the interest of overall system efficiency and integrity…." *Fintiv*, IPR2020-00019, Paper 11 at 14-15 (addressing factor 6). This Petition falls into that category. As described above, the Chapman and Laaksonen references each taught the intermediate hardmask layer and etching steps that the '097 patent describes and claims as the purported invention, including the three claimed etching steps that were missing from the art considered during prosecution. In combination with a trio of other references describing known features and techniques, Chapman and Laaksonen provide the foundation for two separate sets of combinations that render each of the '097 patent's 17 claims obvious. The quantity and quality of the cited prior art in this Petition support institution.

IX. CONCLUSION

Claims 1-17 of the '097 patent are unpatentable.

Dated: August 20, 2021

Respectfully submitted,

/ Tyler R. Bowen /

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CERTIFICATION OF WORD COUNT UNDER 37 CFR § 42.24(d)

Under the provisions of 37 C.F.R. § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter Partes Review* totals 13,966 words, excluding the parts exempted by 37 C.F.R. § 42.24(a).

This word count was made by using the built-in word count function tool in the Microsoft Word software used to prepare the document.

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that true copies of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 6,420,097 and supporting materials (Exhibits and Power of Attorney) have been served this 20th day of August 2021, by Federal Express delivery service on Patent Owner at the correspondence address for the attorney of record for the '097 patent shown in USPTO PAIR:

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